

## Selected Publications and Patents for **Thomas J. Sheffler**

### Recent

Thomas J. Sheffler. *Design of a Switch-Level Analog Model for Verilog*. Proceedings of 2008 IEEE International Behavioral Modeling and Simulation Conference - BMAS 2008.

Thomas J. Sheffler. *AMS Verification and Moore's Law...solutions for 45nm and beyond*. DAC 2008 AMS Verification Panel sponsored by Synopsys.

Thomas J. Sheffler. *Functional Verification in the Presence of Linear Analog Circuits*. Proceedings of DVCON 2008.

Thomas J. Sheffler. *Mixed-Signal Integration: Functional Verification in the Presence of Linear Analog Components*. Proceedings of DesignCon 2008.

Thomas J. Sheffler, Kathryn M. Mossawir and Kevin D. Jones. *PHY Verification - What's Missing?* Proceedings of DVCon 2007.

Thomas J. Sheffler, Kathryn M. Mossawir and Kevin D. Jones. *PHY Verification - Still an Open Problem*. Proceedings of DesignCon 2007.

Thomas J. Sheffler. *Implications of a Configuration Based Verification Environment*. CDNLive 2006.

### Journal Articles

Siddhartha Chatterjee, John R. Gilbert, Leonid Oliker, Robert Schreiber and Thomas J. Sheffler. *Algorithms for Automatic Alignment of Arrays*. J. Parallel and Distributed Computing. Vol. 38. N 2. (1996)

### Books

Thomas J. Sheffler. *The Amelia Vector Template Library*. In Parallel Programming using C++, pages 43-90. MIT Press, 1996.

### Conferences

Thomas J. Sheffler, Robert Schreiber, William Pugh, John R. Gilbert and Siddhartha Chatterjee. *Efficient distribution analysis via graph contraction*. International Journal of Parallel Programming. 1996 December; 24 (6): 599-620.

Thomas J. Sheffler and Siddhartha Chatterjee,. *An Object-Oriented Approach to Nested Data Parallelism*. In Proceedings of the Fifth Symposium on the Frontiers of Massively Parallel Computation, IEEE, Feb., 1995.

Thomas J. Sheffler, Robert Schreiber, John R. Gilbert and Siddhartha Chatterjee. *Aligning parallel arrays to reduce communication*. In Proceedings of the Fifth

Symposium on the Frontiers of Massively Parallel Computation, IEEE, Feb., 1995. Page(s):324 - 331 (A full version of this paper available as Xerox PARC Technical Report CSL-93-7).

Siddhartha Chatterjee, John R. Gilbert, Robert Schreiber and Thomas J. Sheffler. *Array Distribution in Data-Parallel Programs*. Proceedings of the 7th International Workshop on Languages and Compilers for Parallel Computing. 1994. 76-91.

Thomas J. Sheffler. *Implementing the Multiprefix Operation on Parallel and Vector Computers*. Proceedings of the 1993 Symposium on Parallel Algorithms and Architectures (SPAA 93). Velen, Germany. Pages: 377-386.

Thomas J. Sheffler and Randal E. Bryant. *An Analysis of Hashing on Parallel and Vector Computers*. Proceedings of the 1993 International Conference on Parallel Processing.

Thomas J. Sheffler. *Writing Portable Parallel Programs with Match and Move*. Proceedings of the Leeds Second Workshop on Abstract Machine Models for Highly Parallel Computers 1993.

Thomas J. Sheffler and Randal E. Bryant. *Match and Move, an Approach to Data Parallel Computing*. In Proceedings 1992 Advanced Research in VLSI and Parallel Systems.

Thomas J. Sheffler. *Match and Move: Parallel Constructs for Sparse Matrix and Graph Algorithms*. 1993 DIMACS Workshop on Parallel Algorithms for Unstructured and Dynamic Problems.

Randal E. Bryant, Derek Beatty, Karl Brace, Larry Huang and Thomas J. Sheffler. *COSMOS: A Compiled Simulator for MOS Circuits*. In Proceedings 1987 Design Automation Conference.

## Technical Reports

Thomas J. Sheffler. *A Portable MPI-based Parallel Vector Template Library*. RIACS Technical Report RIACS-TR-95.04. March, 1995.

Thomas J. Sheffler, Robert Schreiber, John R. Gilbert and Siddhartha Chatterjee. *Aligning parallel arrays to reduce communication*. Feb. 1995. Xerox PARC Technical Report CSL-93-7.

Thomas J. Sheffler. *A Graph Separator Theorem and Its Application to Gaussian Elimination to Optimize Boolean Expressions for Parallel Evaluation*. CMU Computer Science Technical Report CMU-CS-87-123.

Thomas J. Sheffler. *Match and Move, an Approach to Data Parallel Computing*. CMU Computer Science Technical Report CMU-CS-92-203.

Manpreet Khaira, Gary Miller and Thomas J. Sheffler. *Nested Dissection: A Survey*. CMU Computer Science Technical Report CMU-CS-92-106.

Thomas J. Sheffler. *Implementing the Multiprefix Operation on Parallel and Vector Computers* (full version of conference paper). CMU Computer Science Technical Report CMU-CS-92-173.

Thomas J. Sheffler and Randal E. Bryant. *Work Efficient Hashing on Parallel and Vector Computers*. CMU Computer Science Technical Report CMU-CS-92-172.

## Patents

WIPO WO/2011/022114, Atomic Memory Device. Filing Date 17.06.2010. Publication Date: 24.02.2011. Rambus Inc. Thomas Sheffler, Lawrence Lai, Liang Peng, Bohuslav Rychlik.

WIPO WO/2010/096263. Atomic-Operation Coalescing Technique in Multi-Chip Systems. Publication Date: 26.08.2010. Rambus Inc. Qi Lin, Liang Peng, Craig E. Hampel, Thomas J. Sheffler, Steven C. Woo, Bohuslav Rychlik.

United States Patent 7392492. Multi-Format Consistency Checking Tool. Us Patent Issued on June 24, 2008. Rambus Inc. Qiang Hong, Jing Jiang, Kevin D. Jones, Kathryn M. Mossawir, Thomas J. Sheffler, Paul Wong.

United States Patent 7360187. Mixed mode verifier. US Patent Issued on April 15, 2008. Rambus Inc. Kevin D. Jones, Thomas J. Sheffler, Kathryn M. Mossawir, Qiang Hong, Paul Wong, Jing Jiang.

United States Patent 7039782. Memory system with channel multiplexing of multiple memory devices. US Patent Issued on May 2, 2006. Rambus Inc. Steven Cameron Woo, Ely K. Tsern, Thomas J. Sheffler, Catherine Yuhjung Chen, Abhijit Mukund Abhyankar, Donald C. Stark, Richard M. Barth, Craig E. Hampel, Frederick Abbott Ware, Billy Wayne Garrett, Jr.

United States Patent 6839266. Memory module with offset data lines and bit line swizzle configuration. US Patent Issued on January 4, 2005. Rambus Inc. Richard M. Barth, Ely K. Tsern, Craig E. Hampel, Billy Wayne Garrett, Jr., Steven Cameron Woo, Frederick Abbott Ware, Don Stark, Abhijit Mukund Abhyankar, Catherine Yuhjung Chen, Thomas J. Sheffler.

United States Patent 6708248. Memory system with channel multiplexing of multiple memory devices. US Patent Issued on March 16, 2004. Rambus Inc. Steven Cameron Woo, Ely K. Tsern, Thomas J. Sheffler, Catherine Yuhjung Chen, Abhijit Mukund Abhyankar, Donald C. Stark, Richard M. Barth, Craig E. Hampel, Frederick Abbott Ware, Billy Wayne Garrett, Jr.

United States Patent 6370668. High speed memory system capable of selectively operating in non-chip-kill and chip-kill modes US Patent Issued on April 9, 2002. Rambus Inc. Richard M. Barth, Ely K. Tsern, Craig E. Hampel, Billy Wayne Garrett, Jr., Steven Cameron Woo, Frederick Abbott Ware, Don Stark, Abhijit Mukund Abhyankar, Catherine Yuhjung Chen, Thomas J. Sheffler.

## Patent Applications

International Application No. PCT/US2010/022886 Atomic-operation coalescing technique in multi-chip systems.. International Filing Date 02.02.2010. Qi Lin, Liang Peng, Craig E. Hampel, Thomas J. Sheffler, Steven C. Woo, Bohuslav Rychlik.

USPTO Application: US2007/082891 Verifying Correctness of an Electronic Design Based on Requirements and Conditions of Components of the Electronic Design Pending 11/02/2006. Rambus Inc. Kevin D. Jones, Kathryn M. Mossawir, Thomas J. Sheffler, Vandana Prabhu.

USPTO Application: 2007/0214178 Multi-Project Verification Environment Pending 03/13/2006. Thomas J. Sheffler, Kevin D. Jones, Harlan Samuel Lau, Kathryn M. Mossawir.

USPTO Application: 2007/0079268 Mixed mode verifier. Kevin D. Jones, Kathryn M. Mossawir, Thomas J. Sheffler, Qiang, Hong, Paul Wong, Jing Jiang.

USPTO Application: 20090222253 System and method for Switch-Level Linear Simulation using Verilog. Filing Date: Feb 20, 2009. Rambus Inc. Thomas Jay Sheffler.