

AMS Verification & Moore's Law – Solutions for 45nM and beyond

Tom Sheffler

Rambus[®]

Moore's Law and more transistors:

- **Smaller feature sizes lead to Variability**
 - I_{DS} variation doubles for each technology node below 100nm^[1]
- ***more* transistors, but more *bad* transistors**
 - Digital behavior OK

- [1] H. Masuda, S. Ohkawa, A. Kurokawa, M. Aoki, "Challenge: Variability Characterization and Modeling for 65- to 90-nm Processes," in Proc. IEEE Custom Integrated Circuits Conf., 2005, pp. 593-600.

Digitally-Assisted Analog^[2]

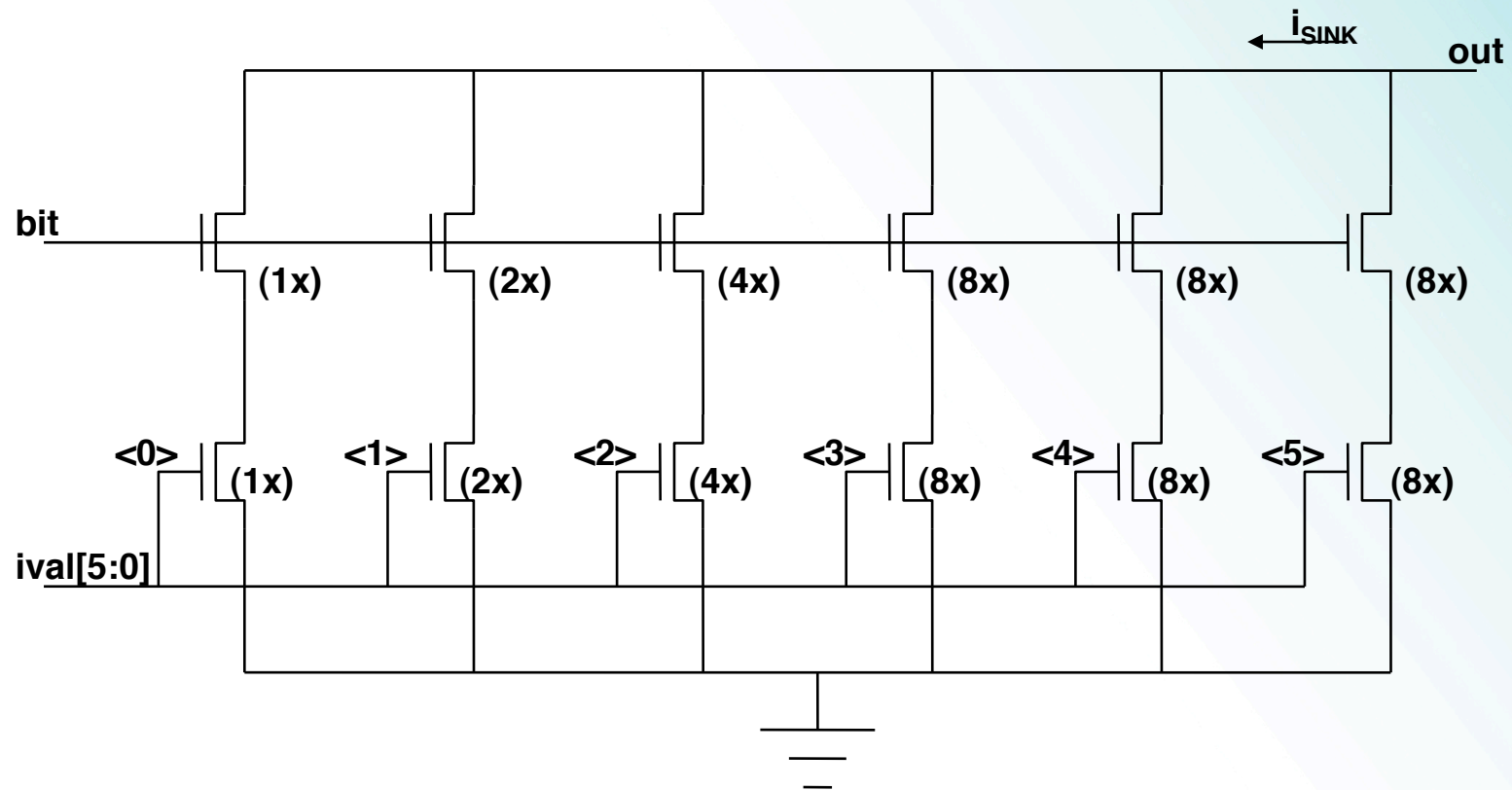
- **Design digitally-adjusted analog circuits.**
 - DAC, iDAC, DCO, Digitally-controlled phase-interpolator
- **Move some complexity to digital domain.**
 - Calibration algorithms in voltage, current, frequency and phase domains
- **We've been doing this a long time ...**

- [2] Boris Murmann – “Digitally Assisted Analog Circuits”

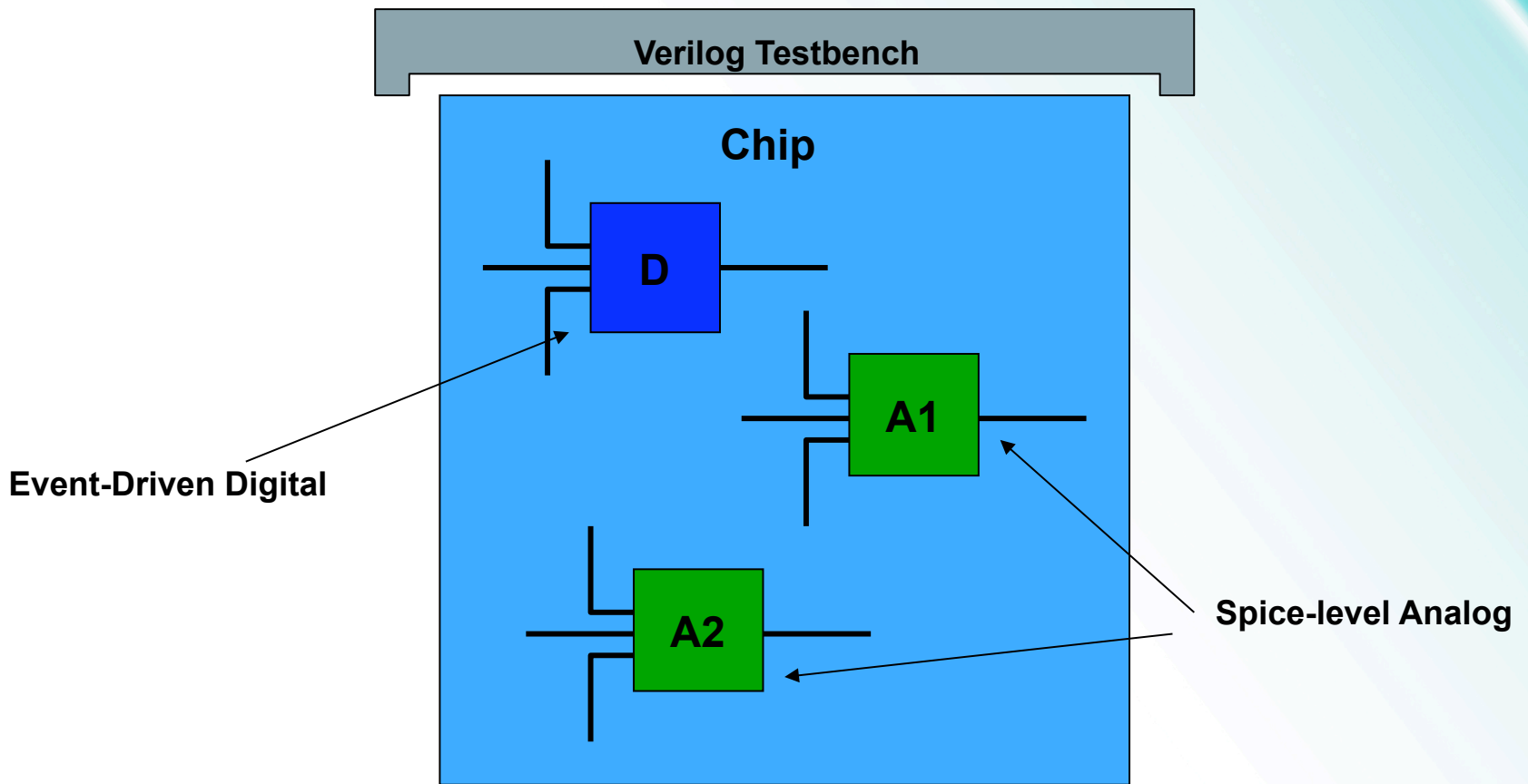
But – all this programmability ...

- **This makes the Verification problem hard!**
- **D/A boundary issues**
 - **Bus Swaps**
 - **Inversion Errors**
 - **Encoding Errors**
 - **Overflow, Underflow**
- **Mixed-signal simulation (Verilog+Spice) is too slow**
 - **And you have to look for the right thing**

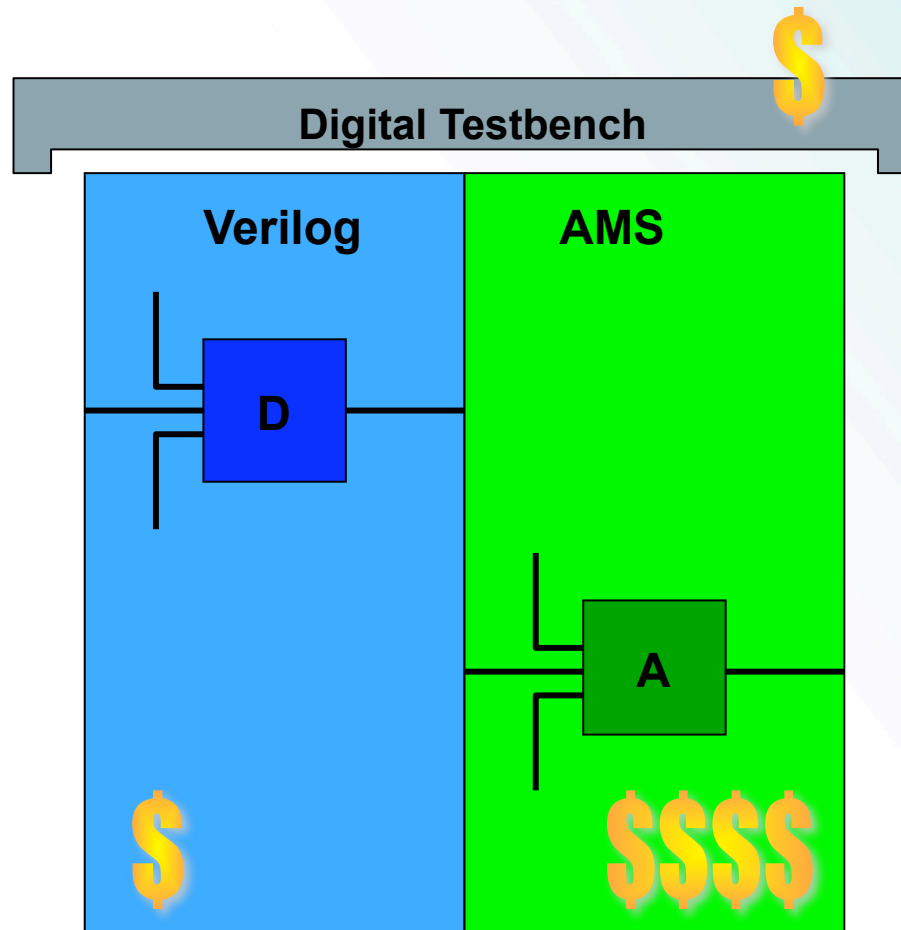
An example digitally-switched analog block



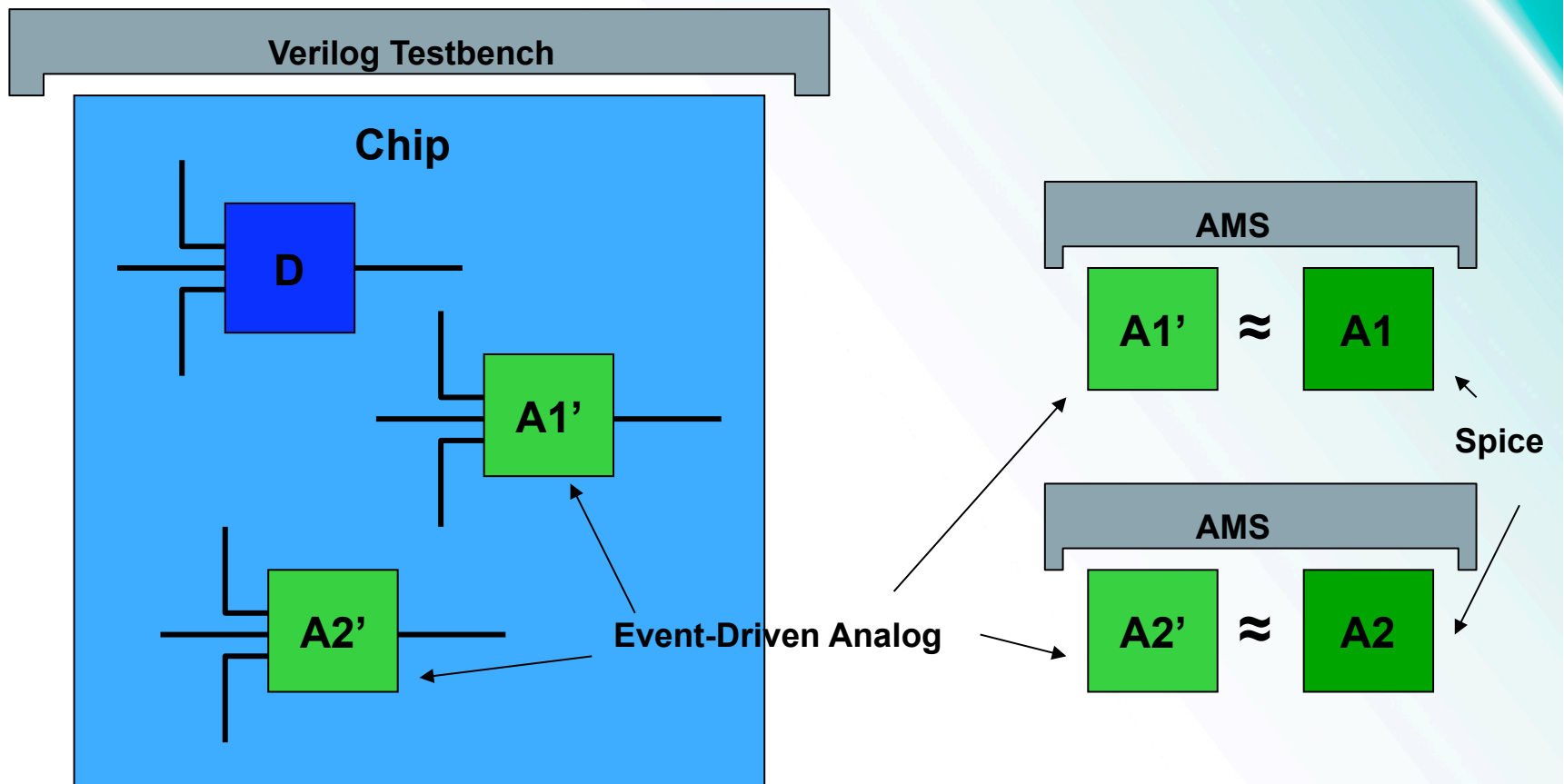
Mixed-Signal Integration: What it is



The price of simulation: license cost (and time)



Hierarchical Verification



End Remarks

- **Digitally-controlled analog pervasive.**
- **Need techniques and tools that scale:**
 - **Functional abstraction of analog**
 - **Composition at the abstraction level**
 - **Tool cost and speed commensurate with digital TB**