

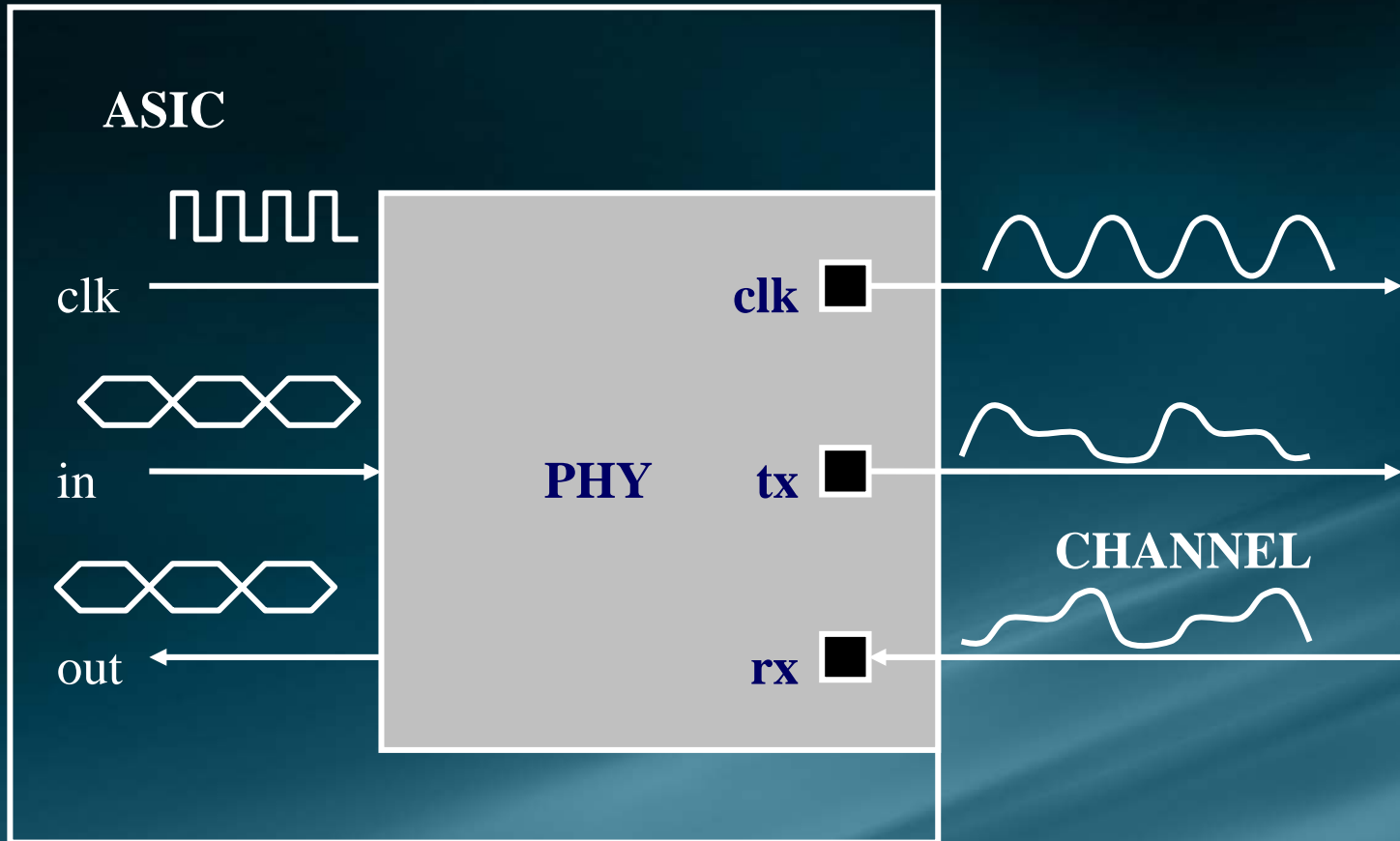


PHY Verification – What's Missing?

February 22, 2007

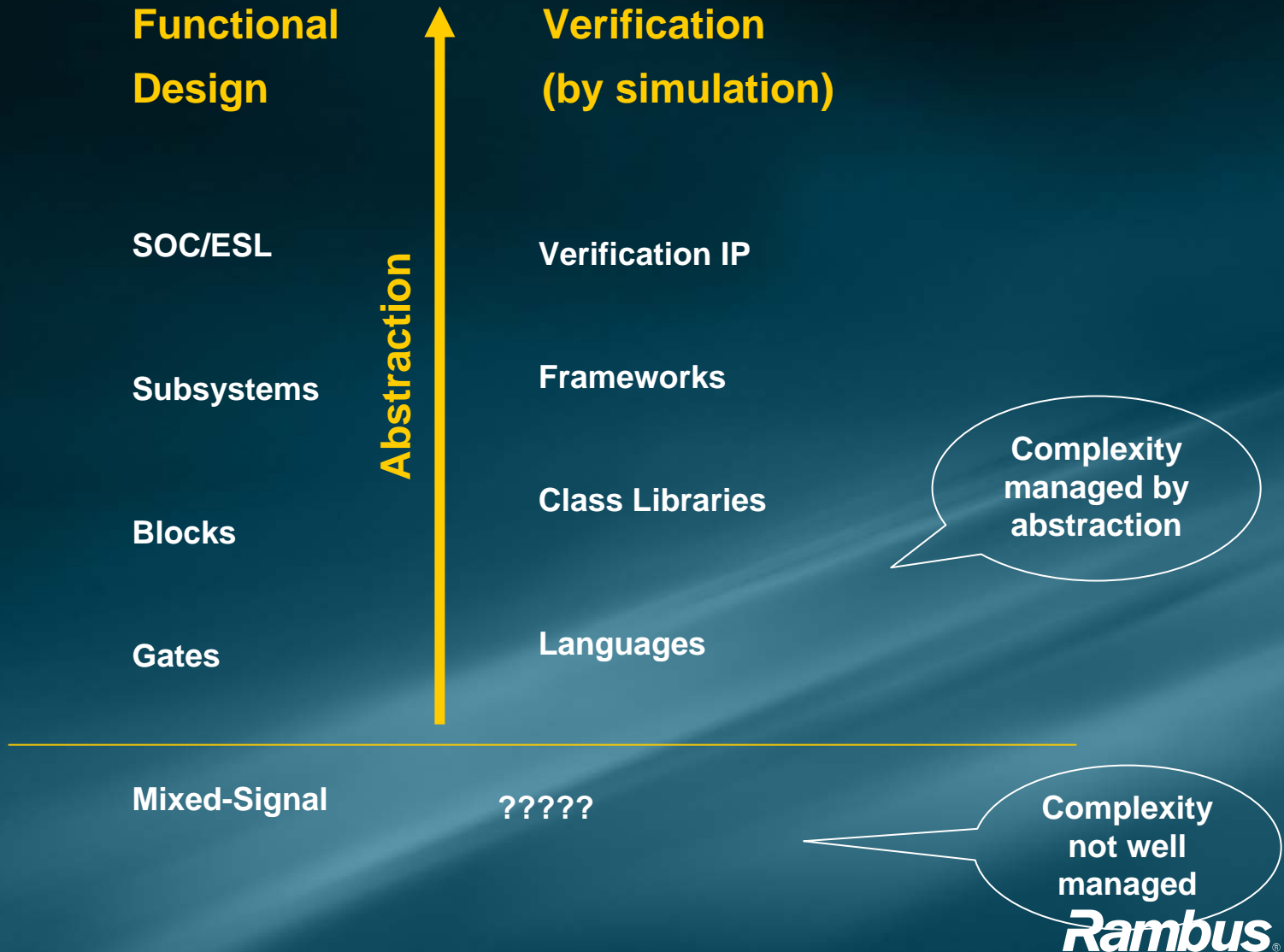
Tom Sheffler
Katy Mossawir
Kevin Jones

What's a PHY?

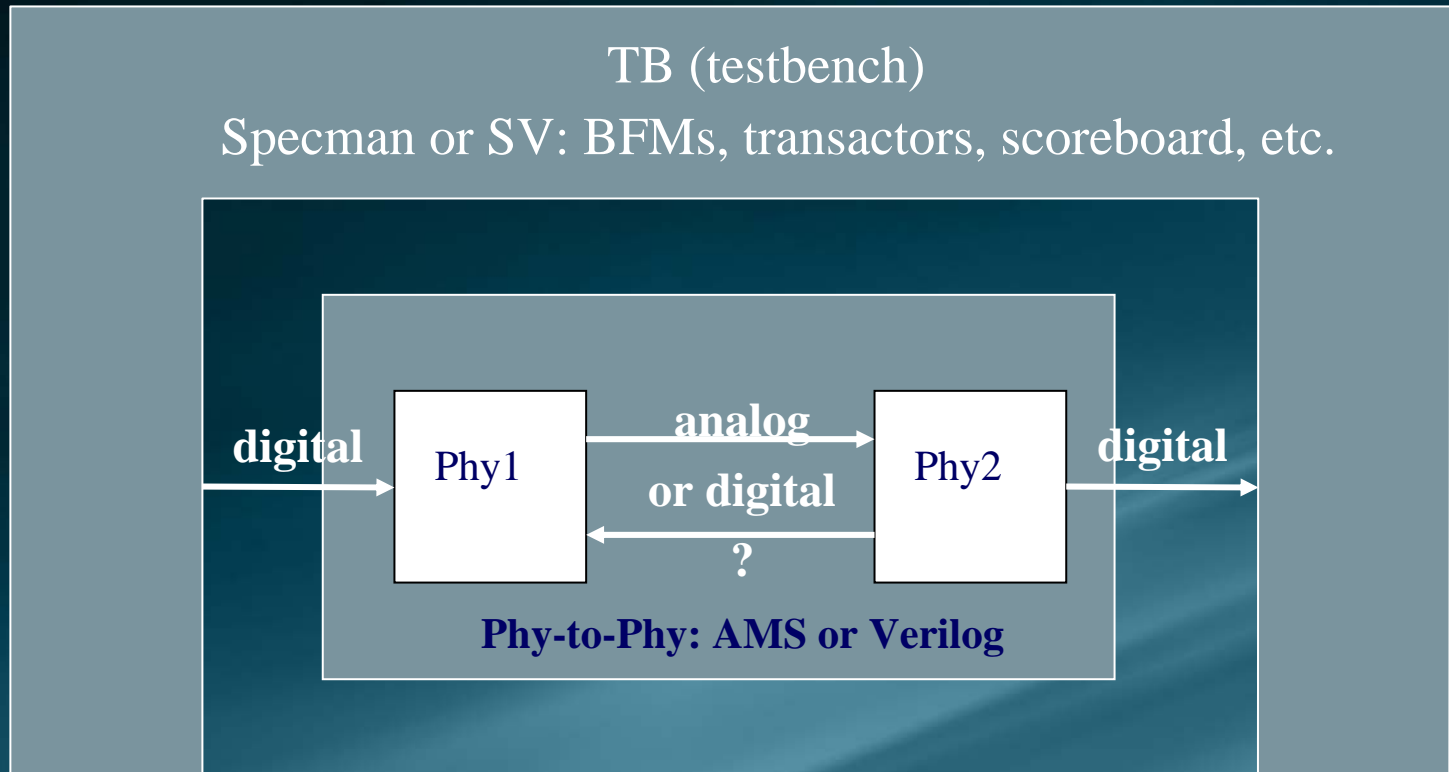


- On-chip logical to Off-chip physical

Managing Integration Complexity

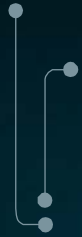


PHY-to-PHY Verification Environment



Organization of this Talk

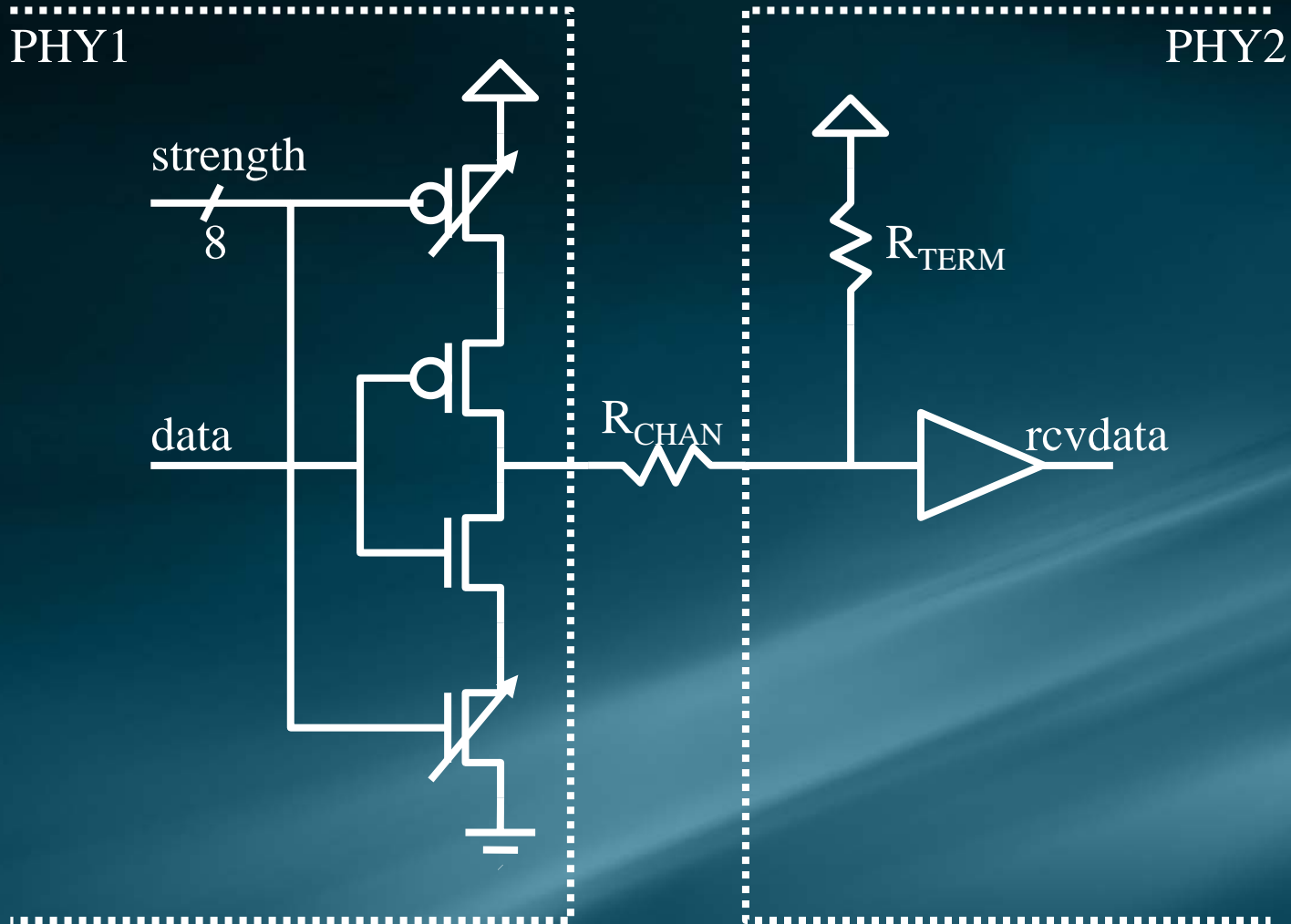
- **Present small examples**
 - **Representational archetypes**
- **Discuss verification challenges**
- **Raise question of ensuring correctness**



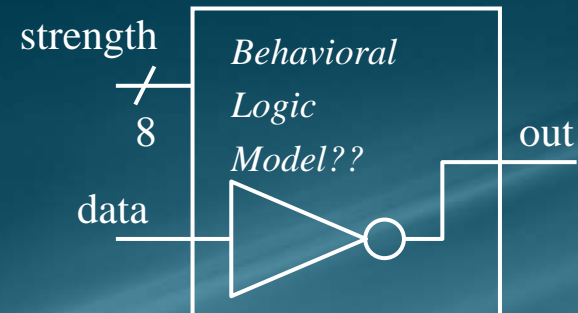
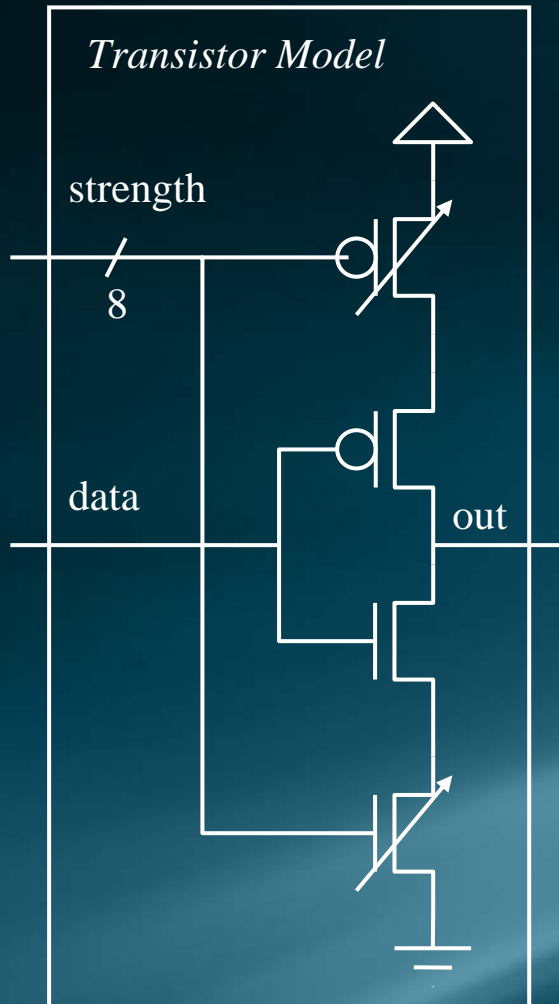
Example 1:

Signal Conditioning

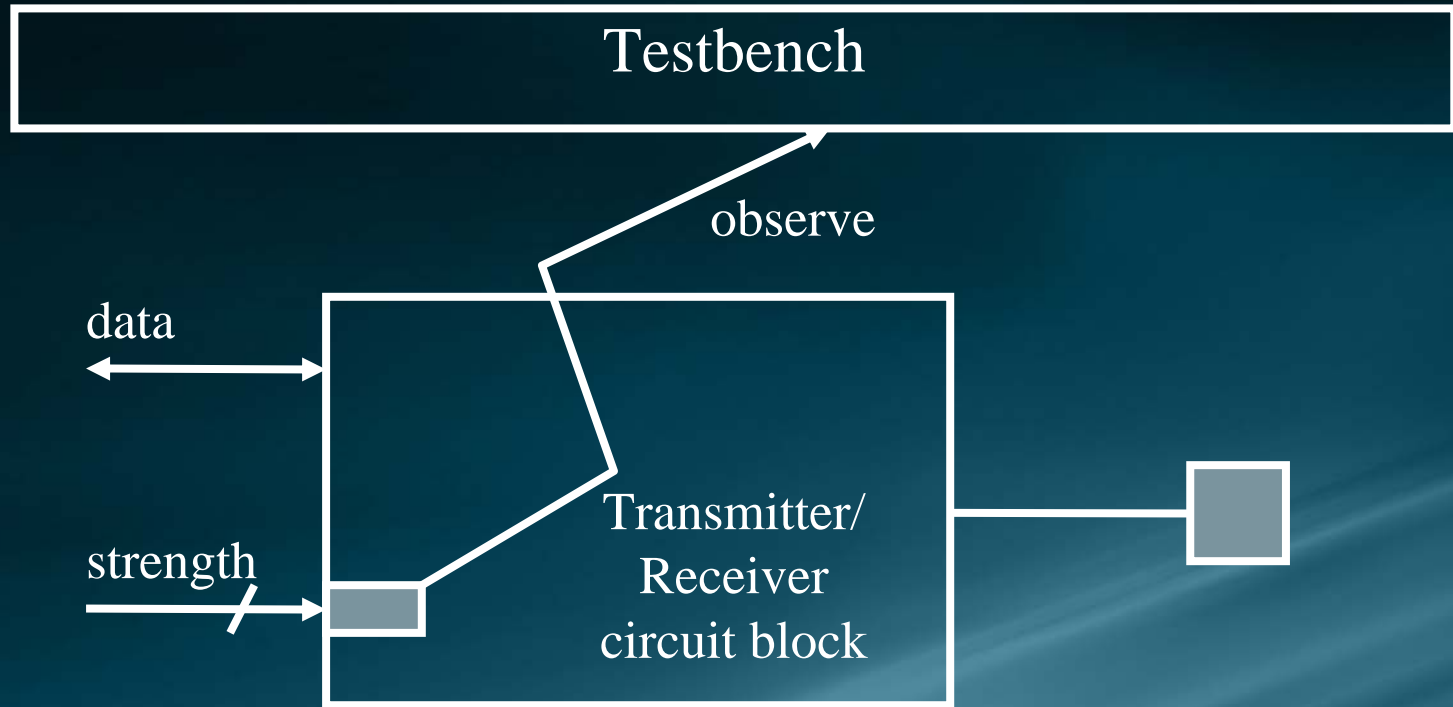
Programmable Strength Driver



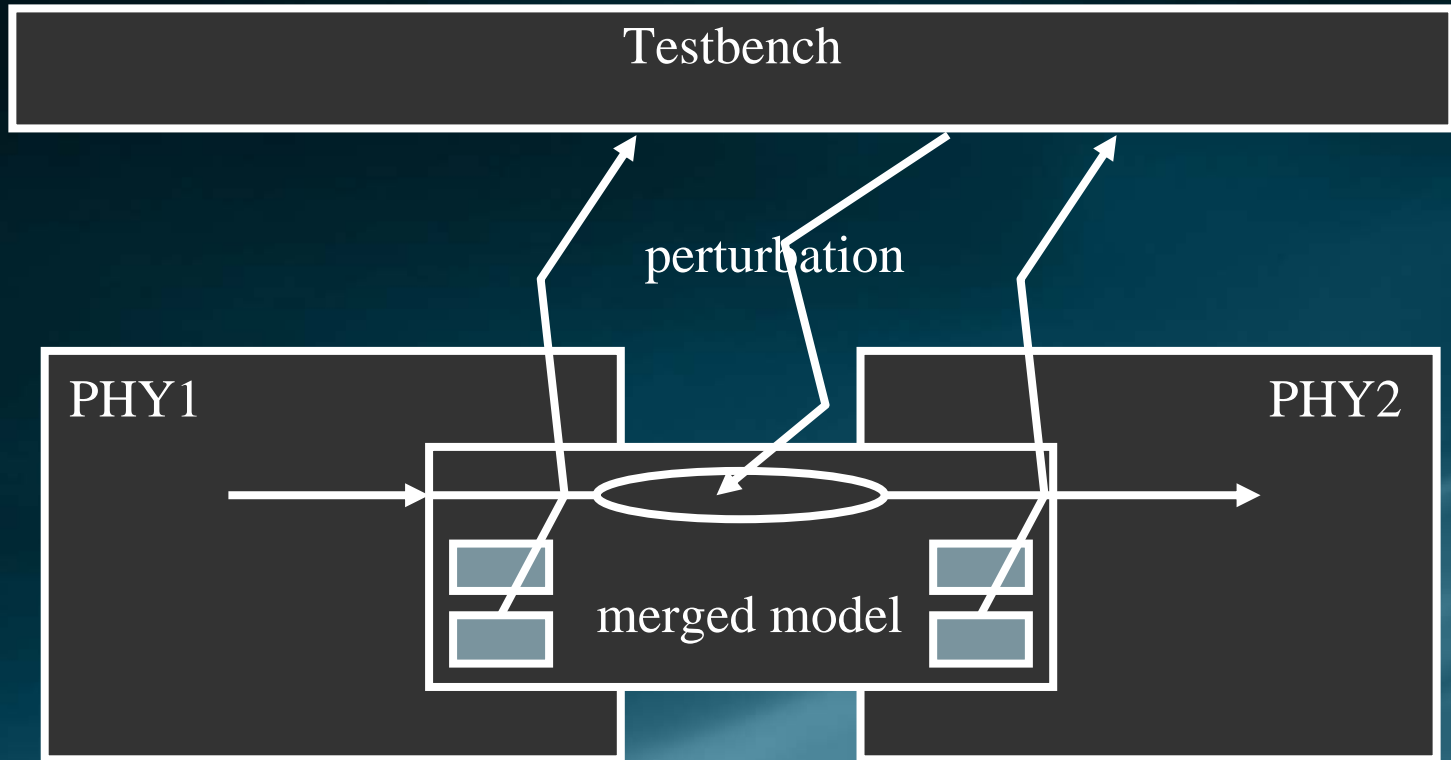
Behavioral Substitution



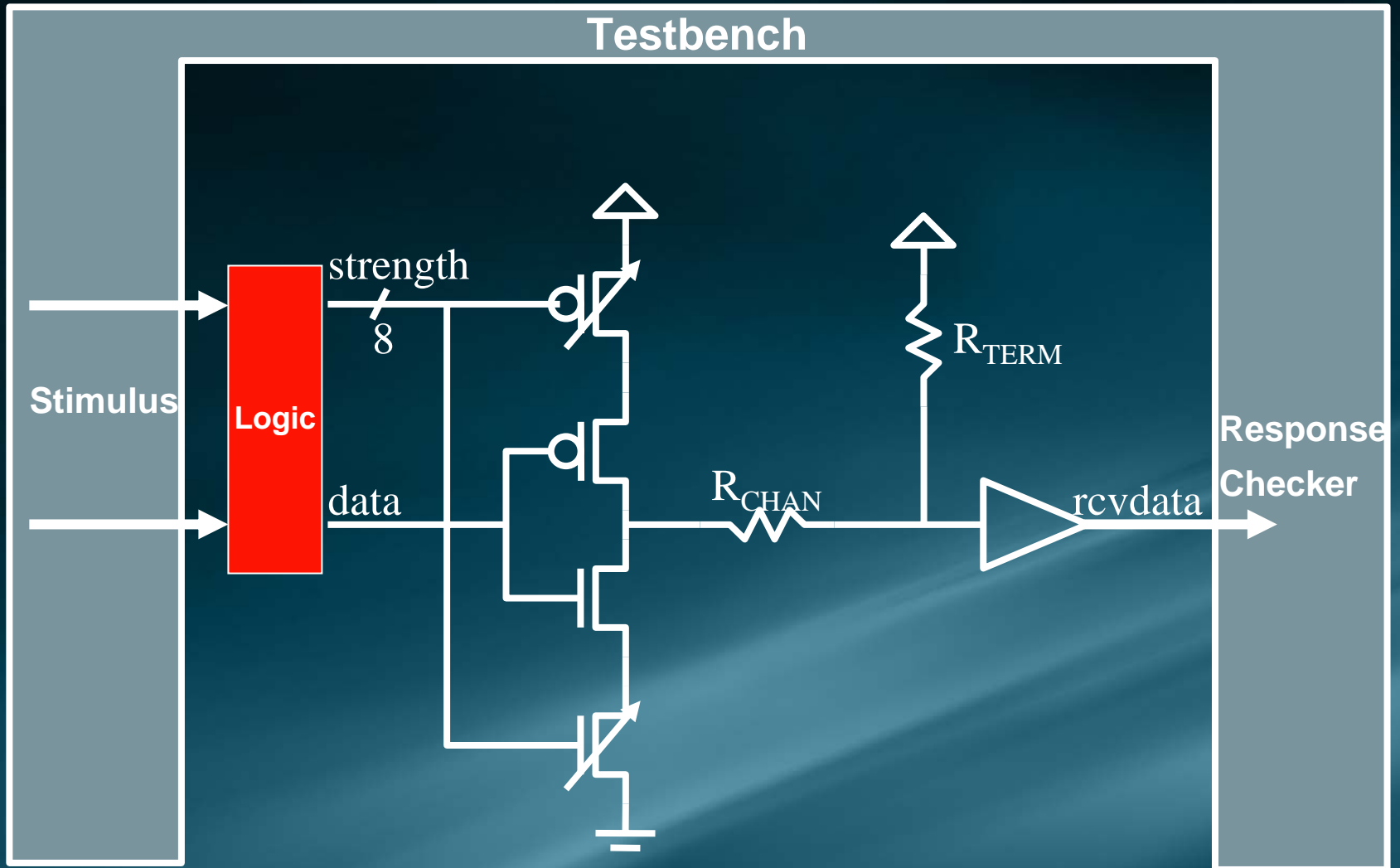
Direct Observation



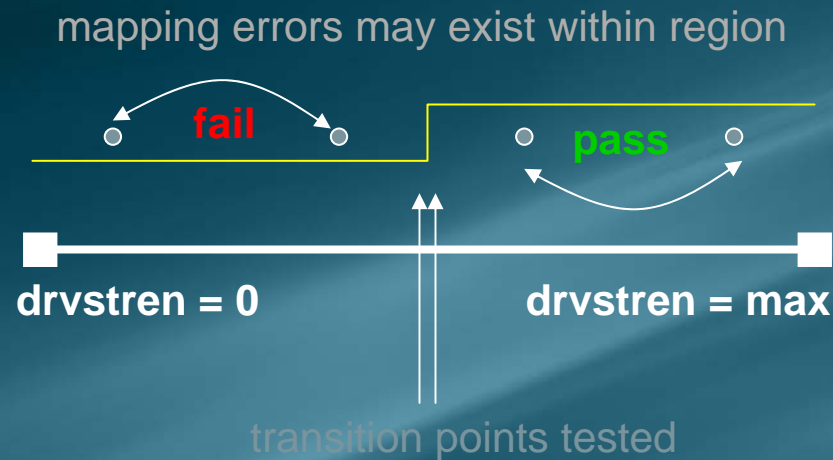
Logical Channel Model



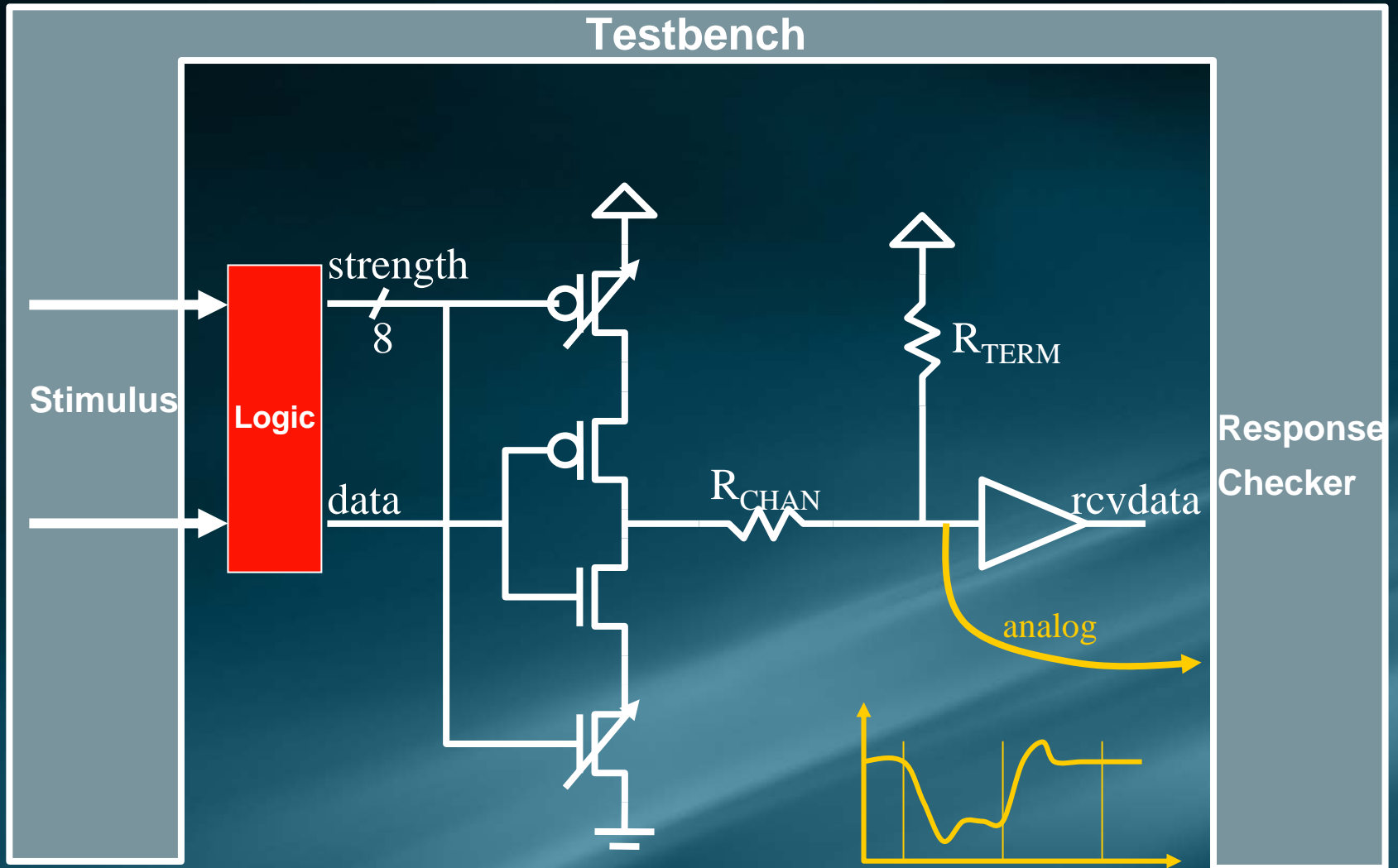
Mixed-Signal Simulation



- **Typical Verification Procedure**
for each `drvstren`:
check `rcv == data ??`



Analog Response Checker

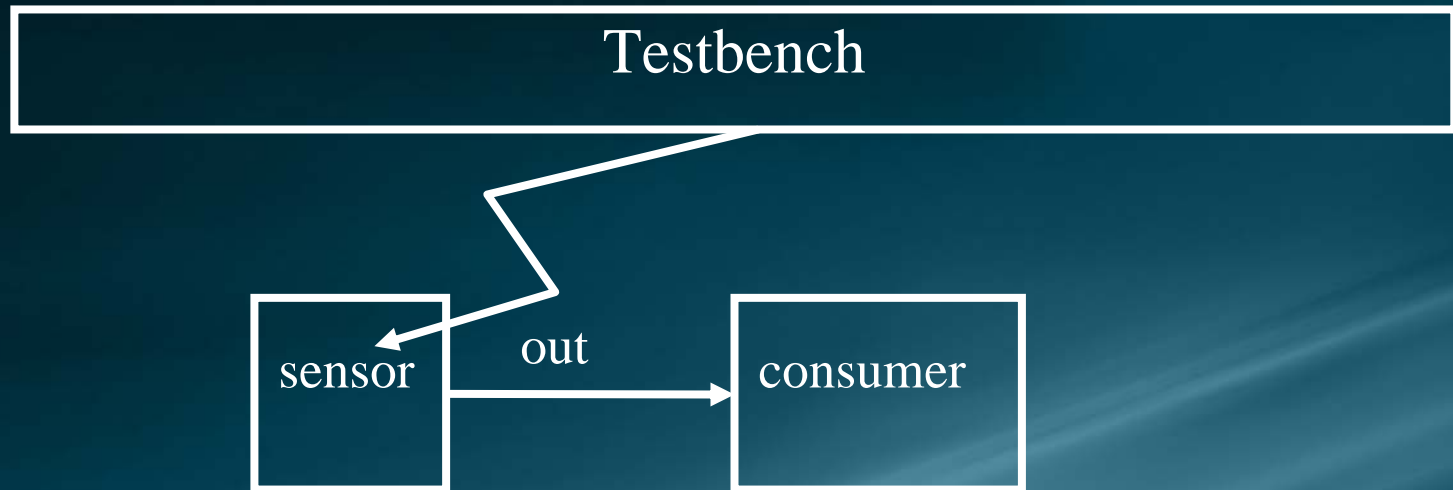




Example 2:

Environment Detection

Sensor



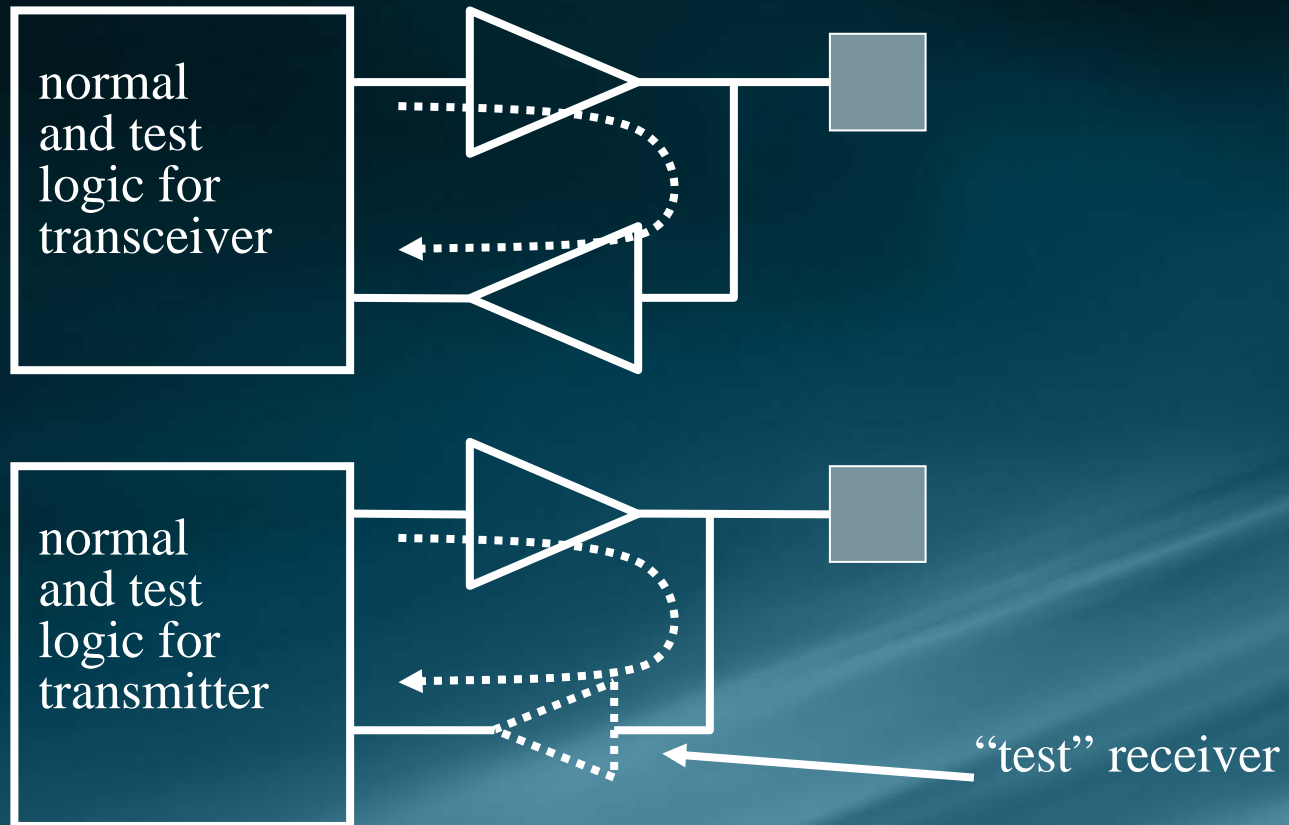
- **Modeling of environmental conditions**
 - **Temperature**
 - **Line characteristics**
- **Means to inject logical effect of environmental change**
 - **Testbench to internal node connection**



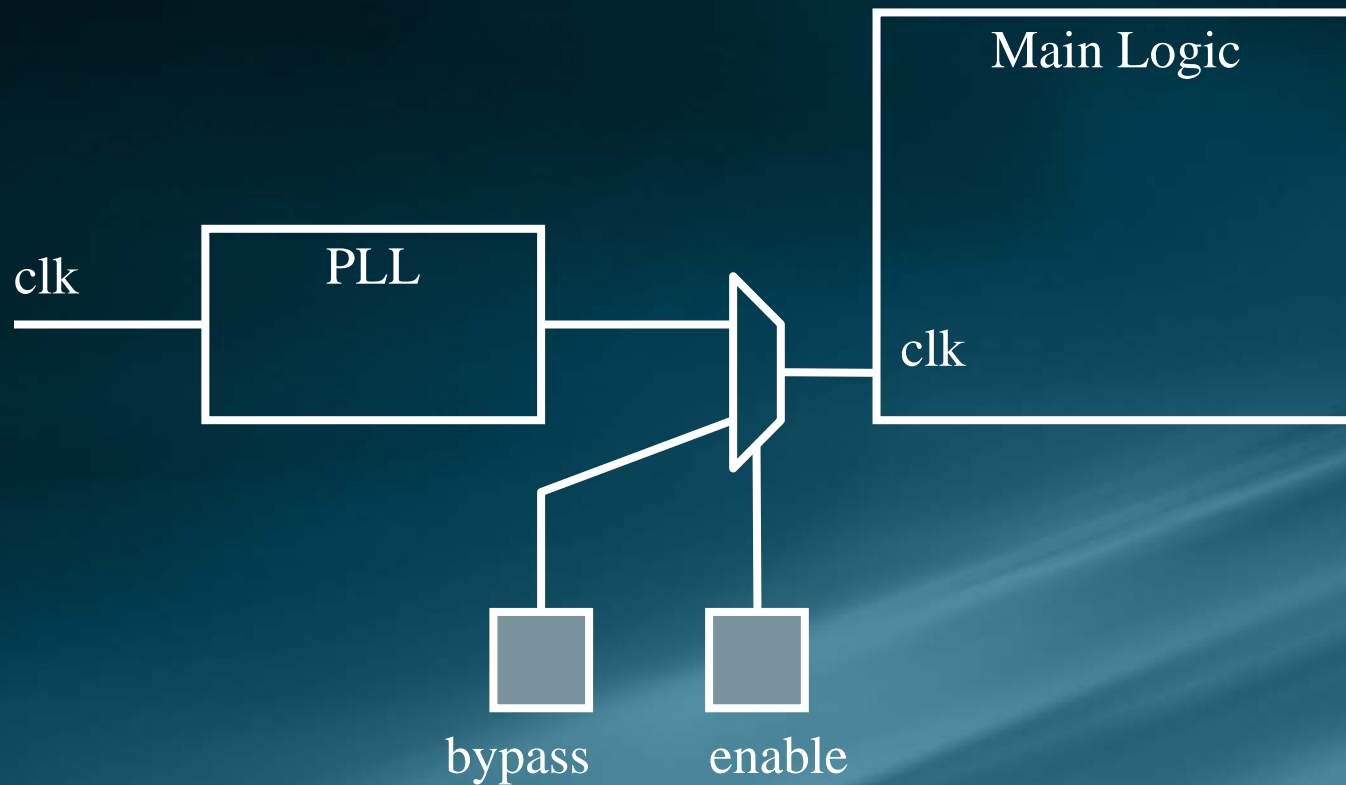
Example 3:

Analog Test

Analog Test



Analog Test

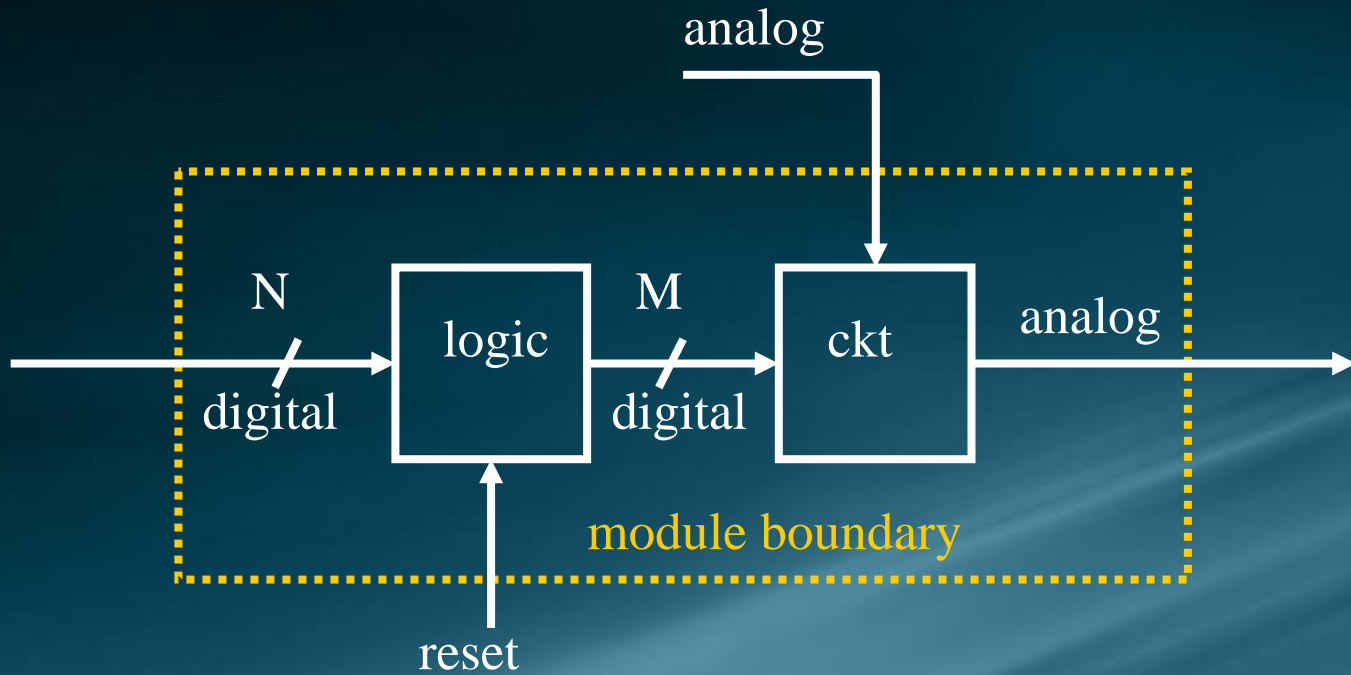




Example 4:

Embedded Logic

Embedded Logic

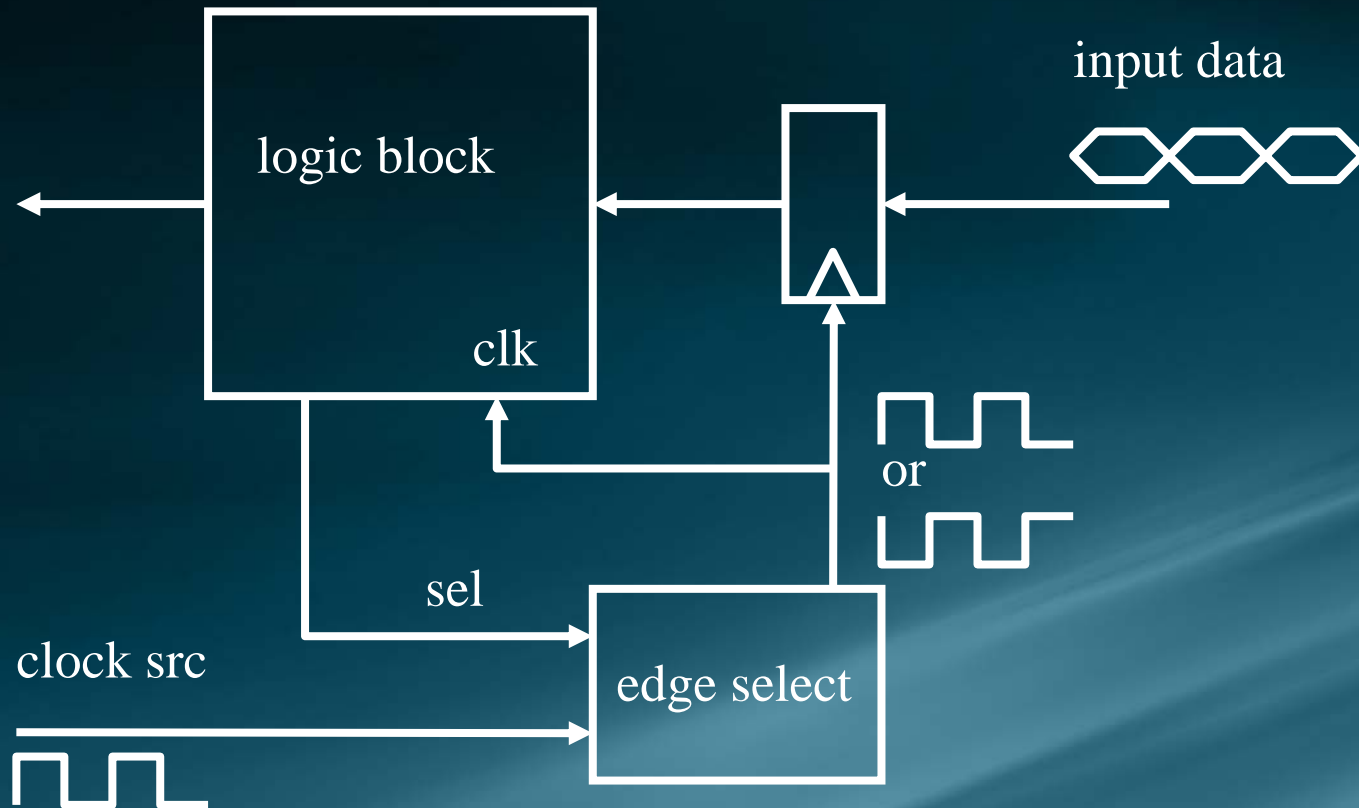




Example 5:

Computed Clock

Computed Clock

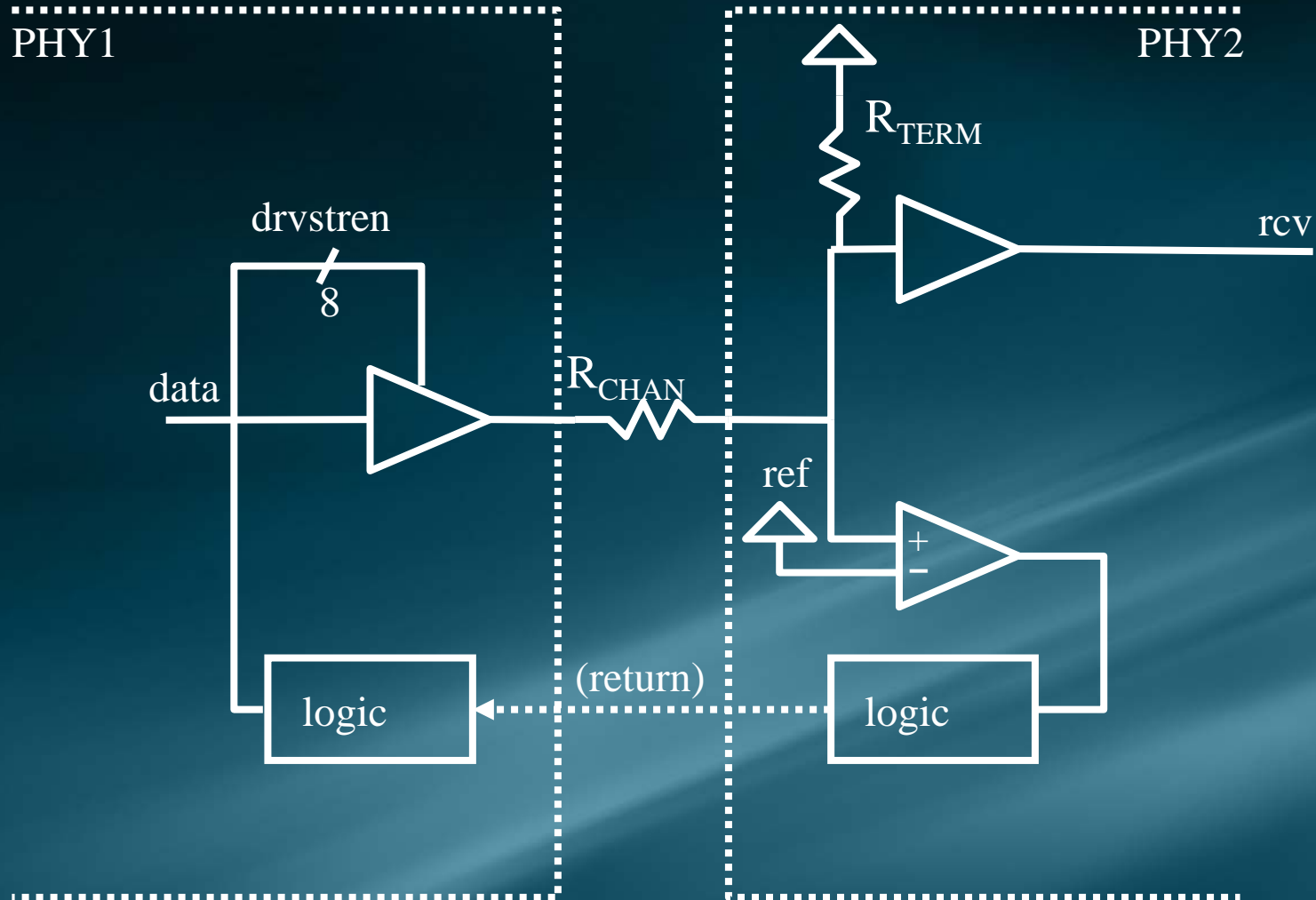




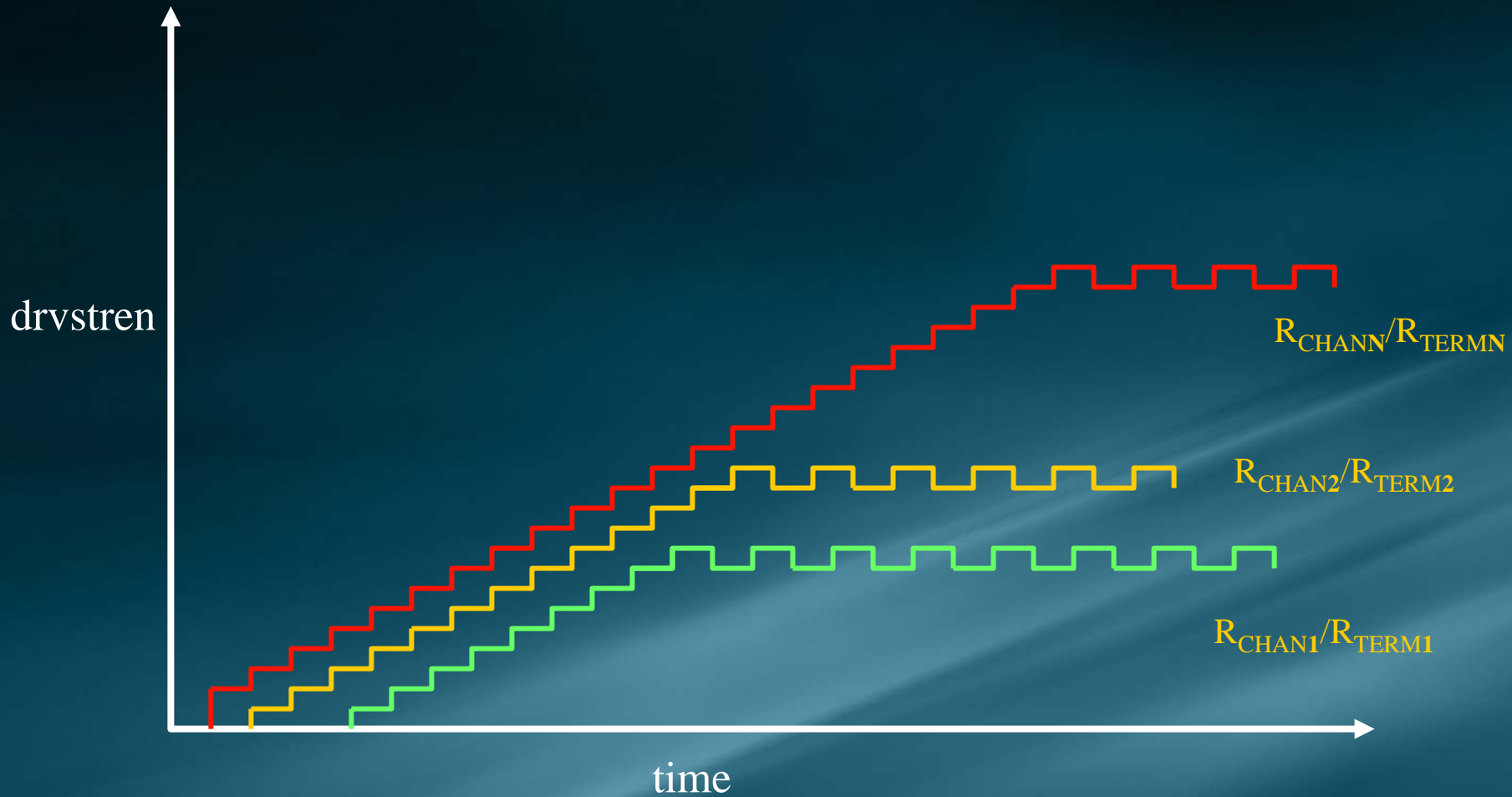
Example 6:

Feedback Control System

Feedback System



Feedback Control System Time Responses




Simulation Lifetime

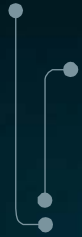
1. Template Expansion
2. Compile
3. Elaborate
4. Simulate
 - 4.1 Model Reset
 - 4.2 GEN
 - 4.3 Model Config
 - 4.4 Reset DUT
 - 4.5 Configure DUT
 - 4.6 Run
 - 4.7 Report
5. Analyze



CRT
Scope



Configuration
Scope



Summary

Summary

- **Design patterns found in PHYs do not fit well with many verification methods**
- **Examples**
 - **Signal Conditioning Circuit**
 - **Environment Detection**
 - **Analog Test**
 - **Embedded Logic**
 - **Computed Clock**
 - **Feedback Control System**
- **Ad-hoc handling of these patterns leads to confusion**

What's Missing?

- **Short-term**
 - Testbench to DUT internals
 - Analog stimulus generation and response checking
 - Analog DFT
 - Configuration variation under testbench control
- **Long-term**
 - New tools and representations to capture intent
 - Multiple design representations
 - Proven correlation

Call-to-Action

- **Systematize design idioms/patterns**
 - **Build a common lexicon**
 - “scoreboard”, “transactor”
 - **Systematize Verification**