



Mixed-Signal Integration: Functional Verification in the Presence of Linear Analog Components

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Tom Sheffler
Rambus Inc.

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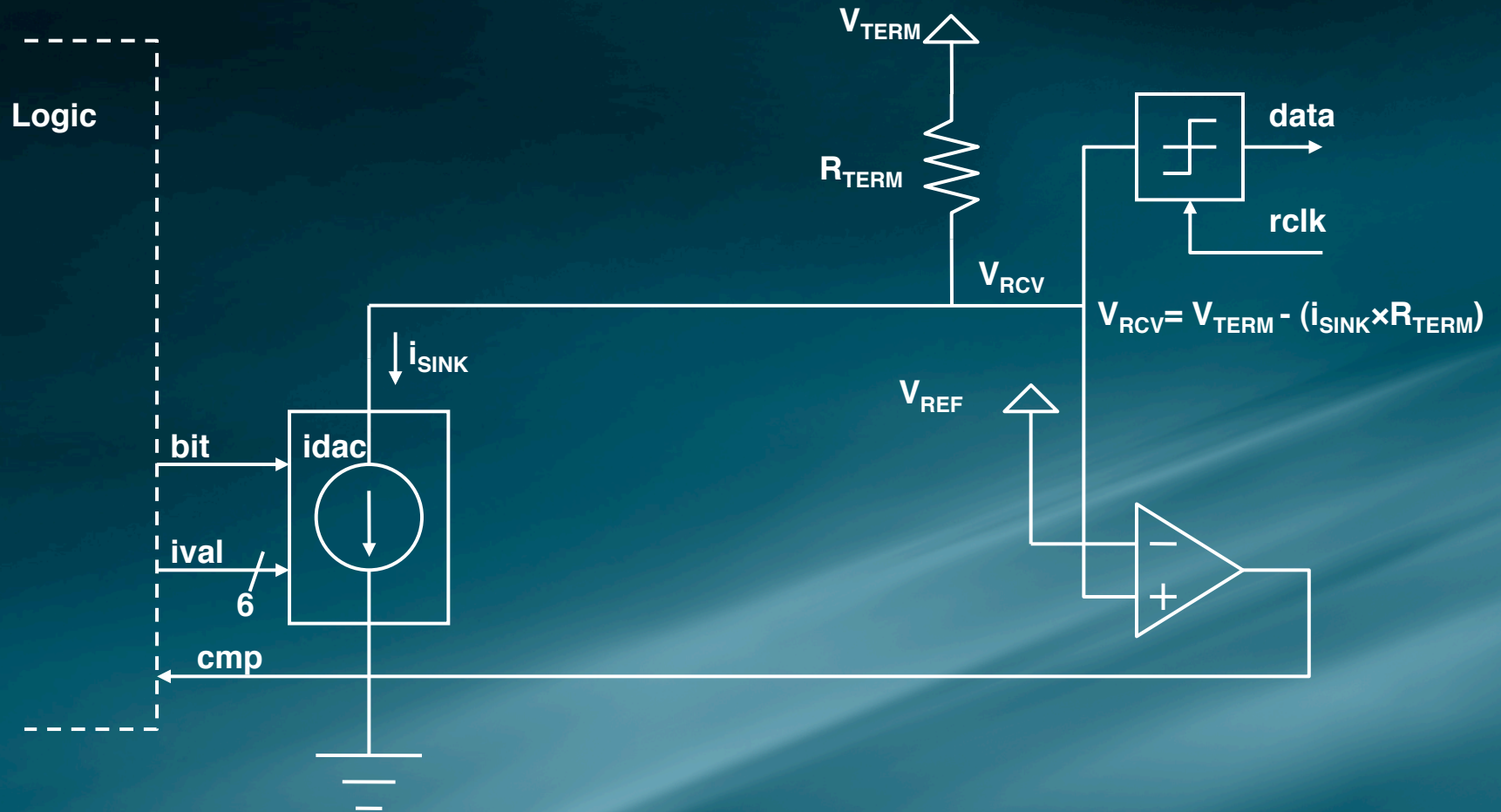
- **Rambus Innovations**
 - **Output Driver Calibration**
 - **On Die Termination Calibration**
 - **Flex-Phase**
 - **Equalization**

- **<http://www.rambus.com/us/patents/innovations>**

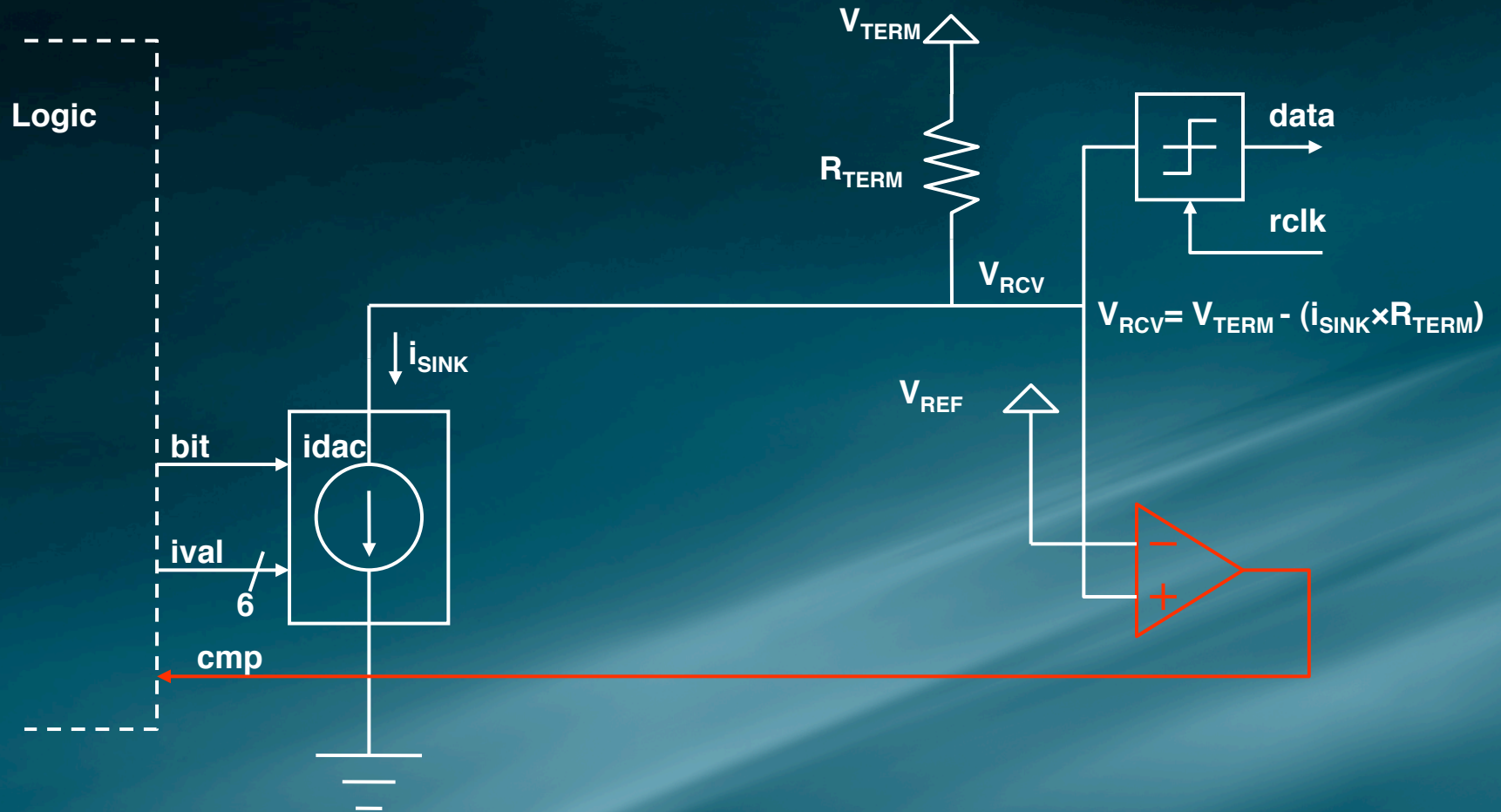
Talk Roadmap

- Explain a mixed-signal subsystem.
- Explain its components.
- Illustrate how D/A boundary errors can be difficult to detect.
- Show a way to model the components, suitable for detecting D/A boundary errors.

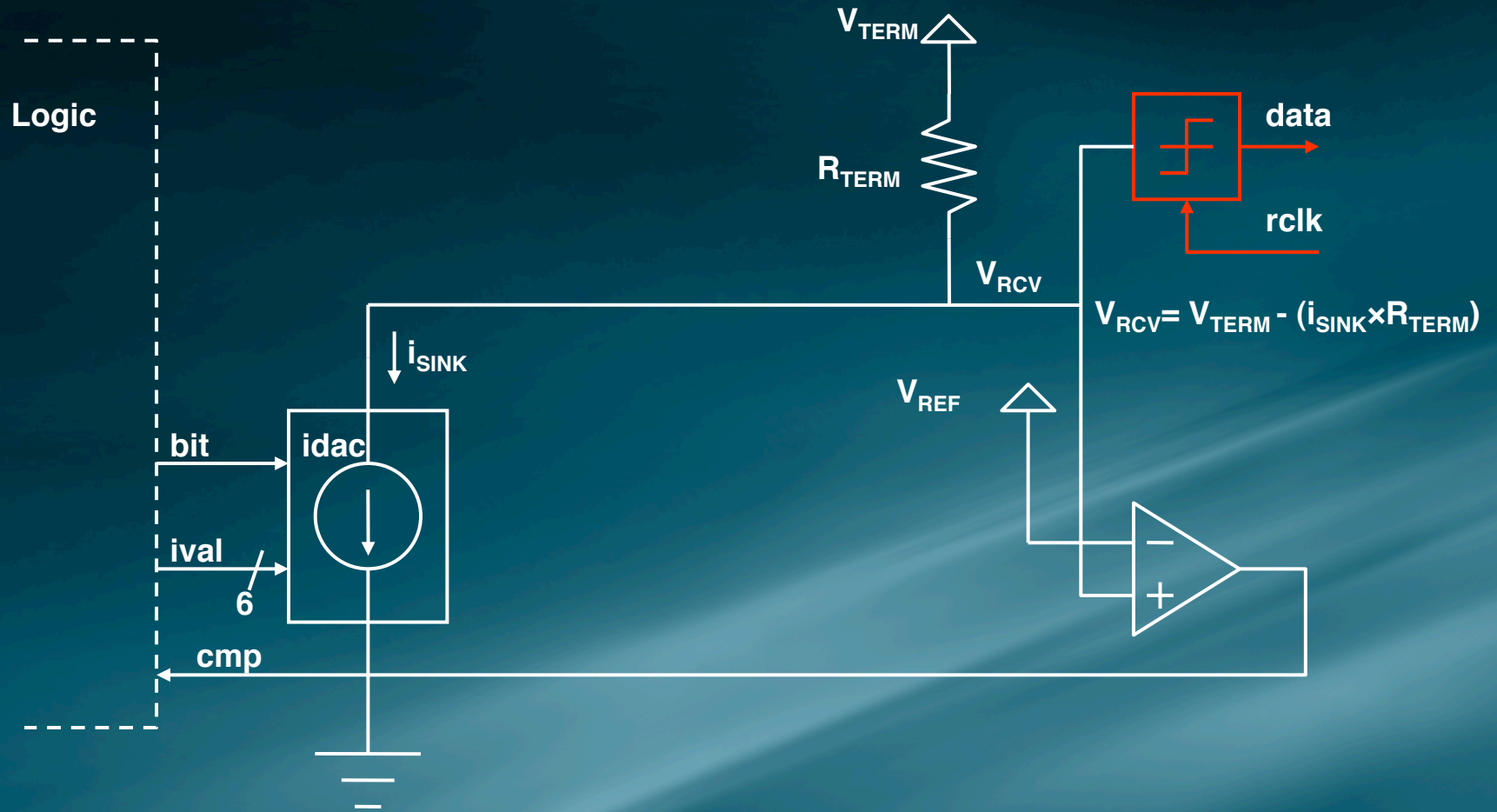
Output Driver with Feedback



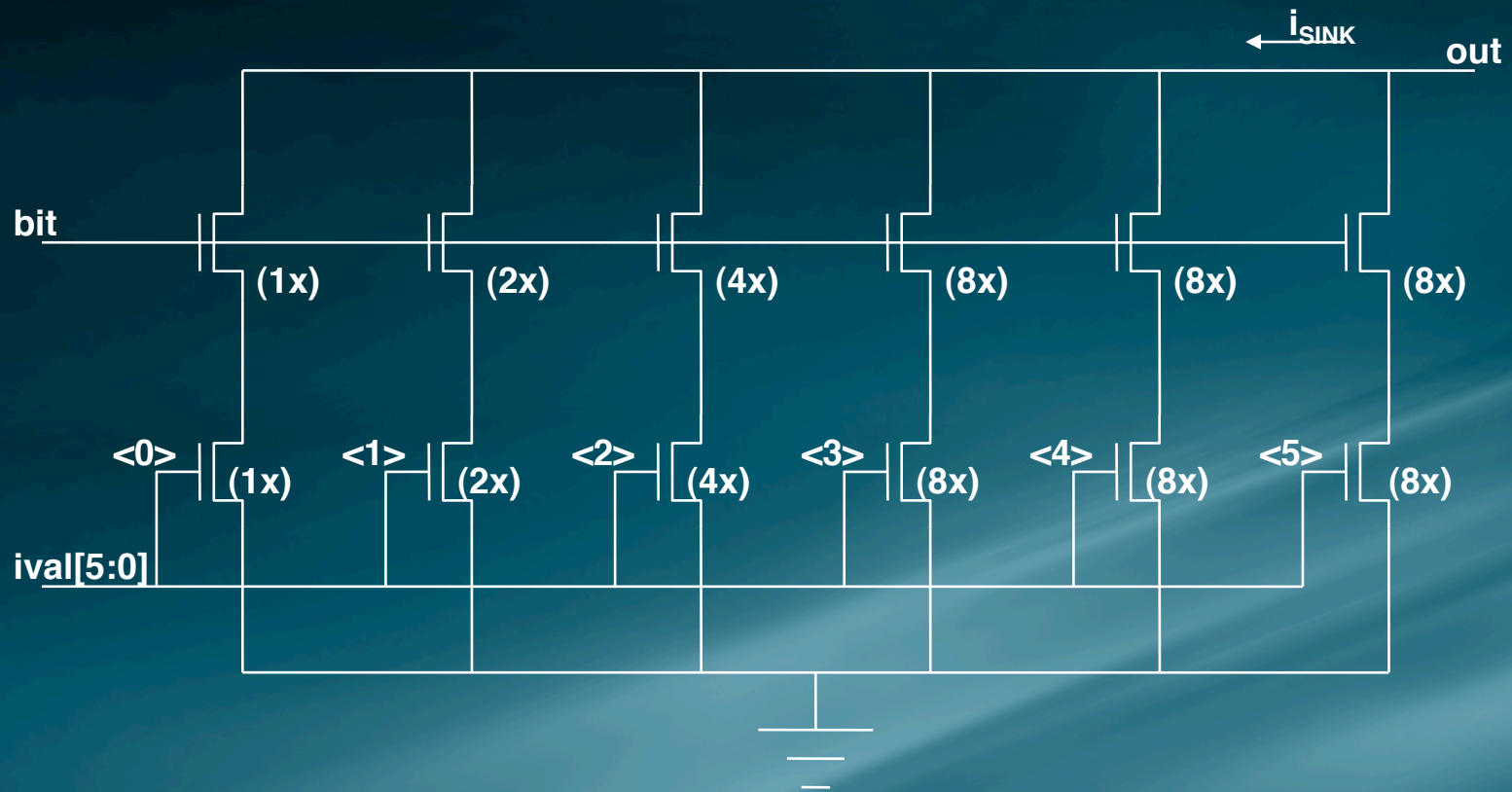
Output Driver with Feedback – Normal



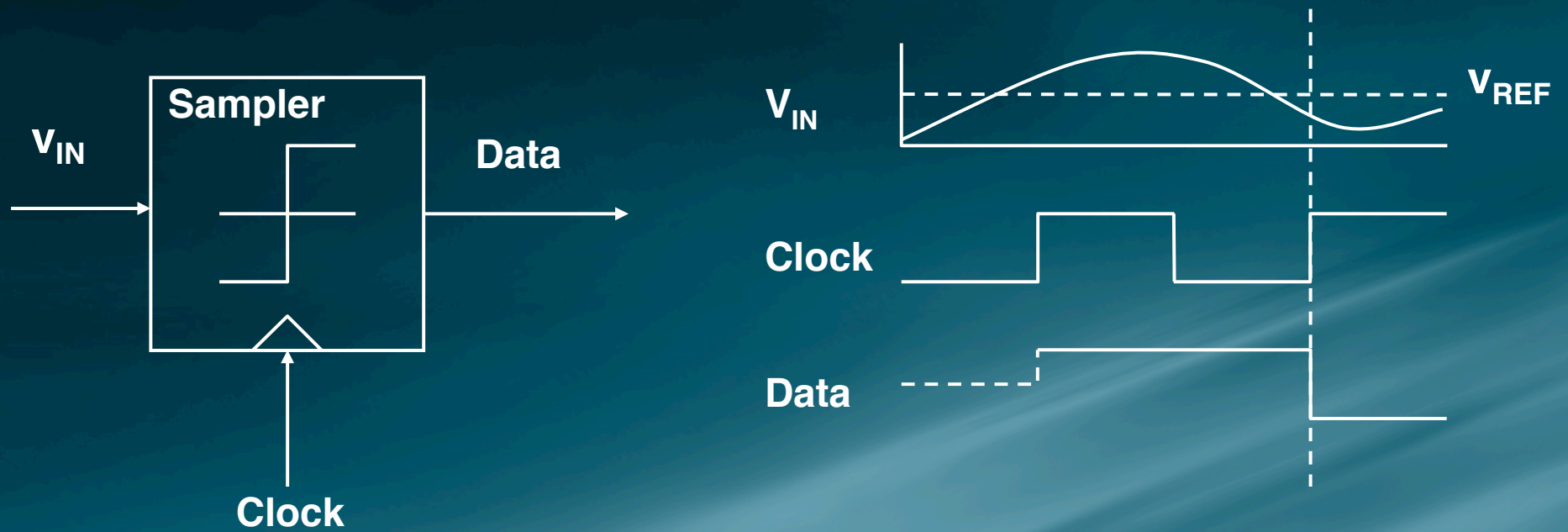
Output Driver with Feedback - Calibrate



IDAC Schematic



Input Sampler



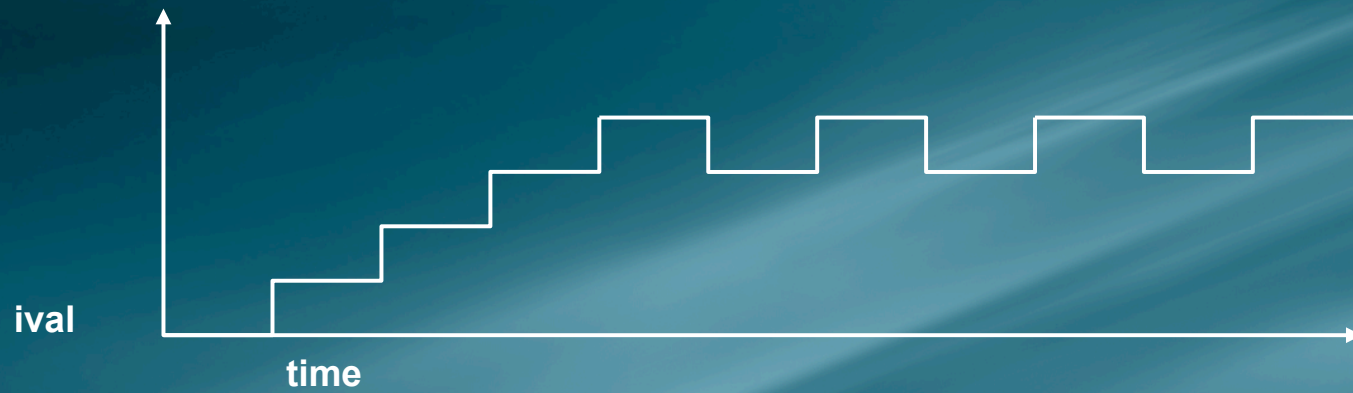
Calibration Algorithm

```
module tracker(input cmp, input clk, input enabled, input reset, output ival);
    reg [4:0] code; initial code = 0;
    reg [5:0] ival; initial ival = 0;
    always @(posedge reset)
        code = 5'b00000;
    always @(posedge clk)
        if (enabled) begin

            // up or down?
            code = code + 1 if (cmp == 1'b0)
;
            else
                code = code - 1;

            // translate to 'thermometer' code
            ival[2:0] = code[2:0]
            ival[3] = integer(code) >= 8;
            ival[4] = integer(code) >= 16;
            ival[5] = integer(code) >= 24;
        end
        delay(settling_time);
    end
endmodule
```

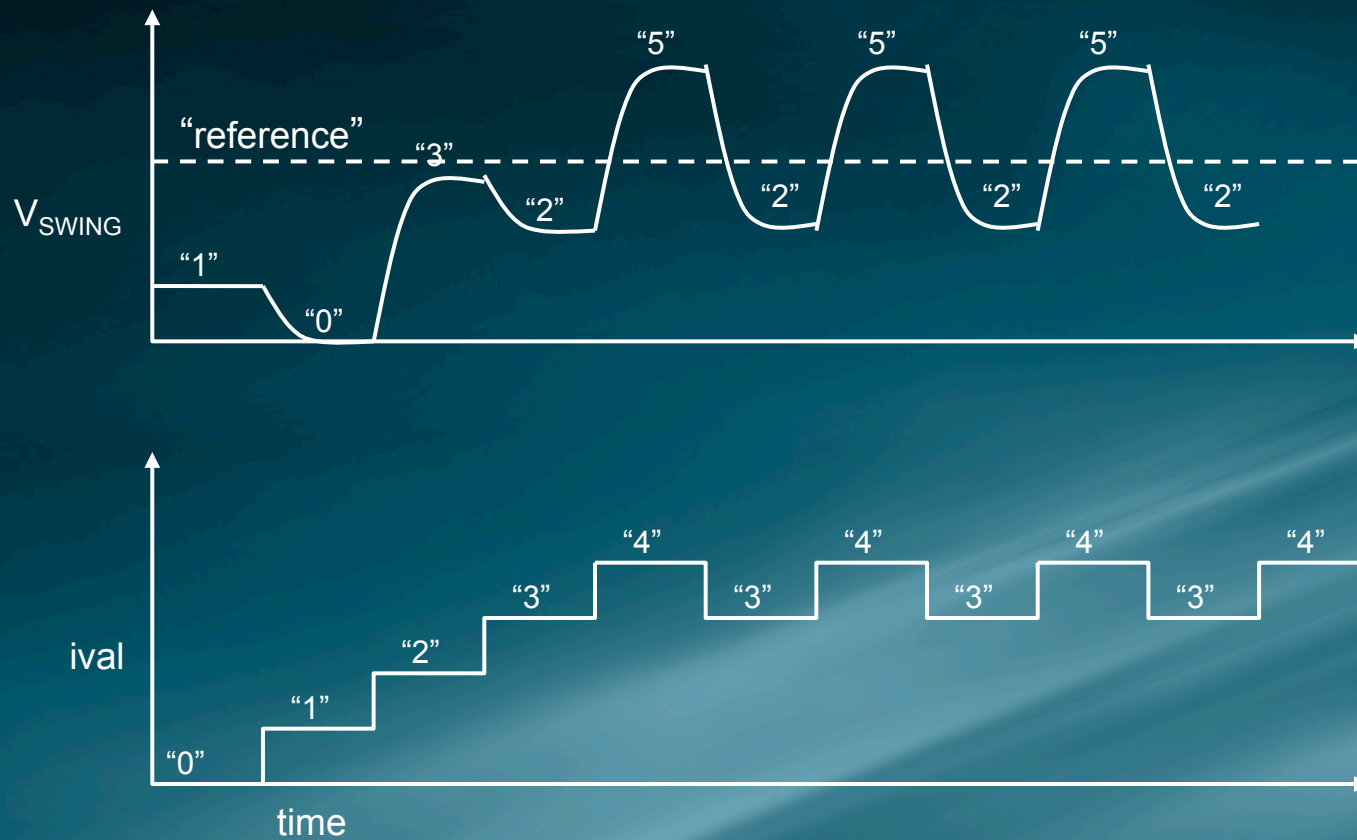
Feedback Tracker Behavior



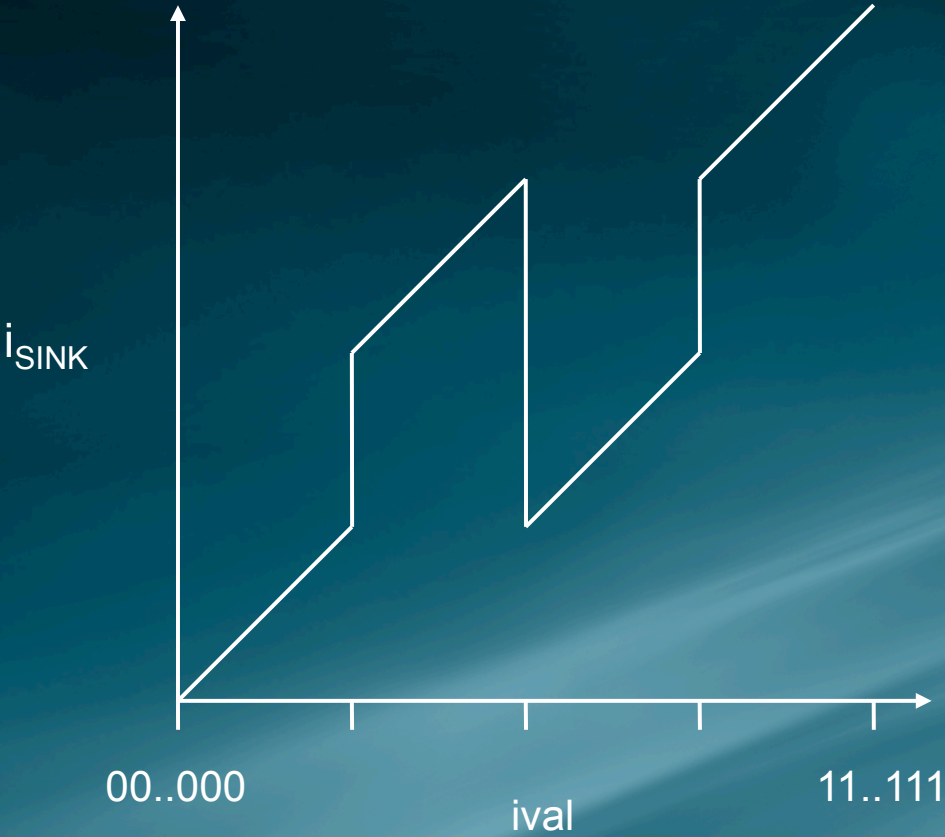
Common Integration Errors

- **Bus Swaps**
- **Inversion Errors**
- **Encoding Errors**
- **Overflow, Underflow**

Tracker Behavior with LSB Inversion

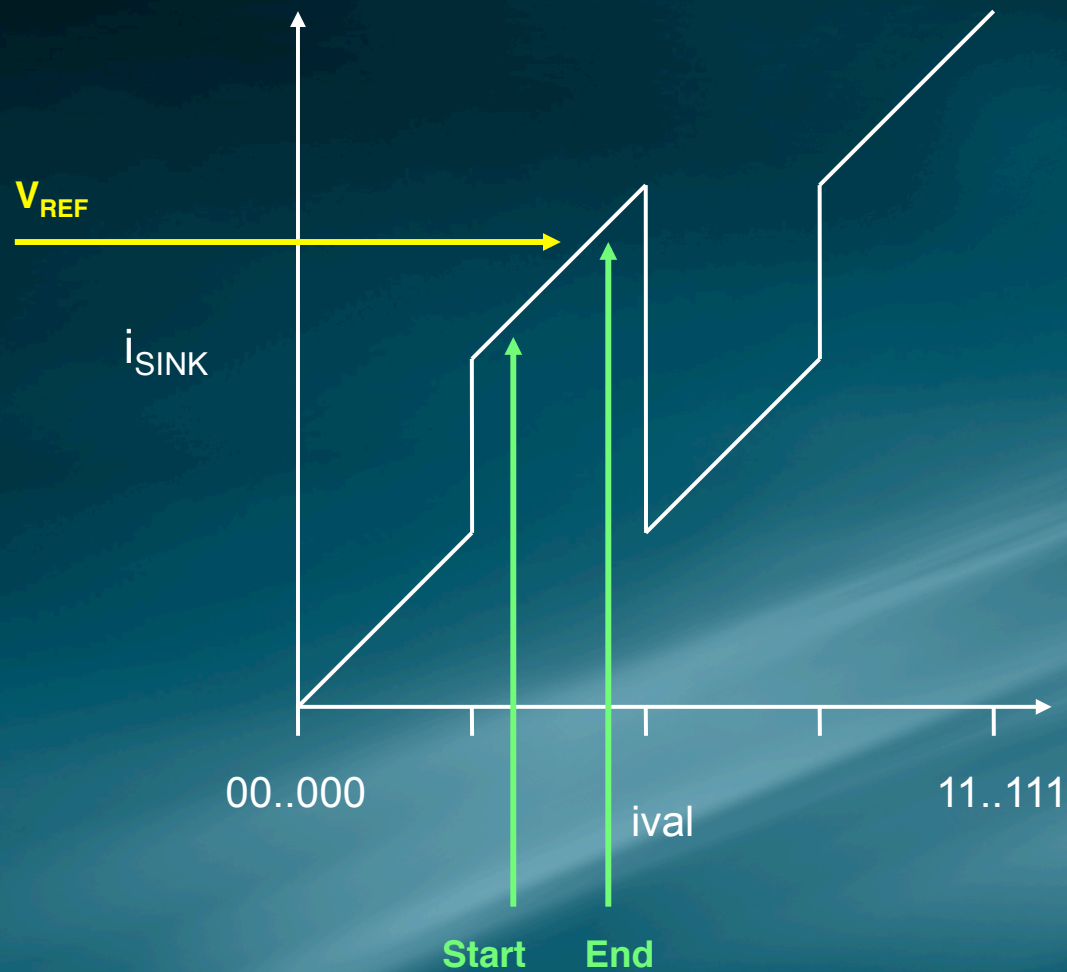


Effective DAC Transfer Function - MSB



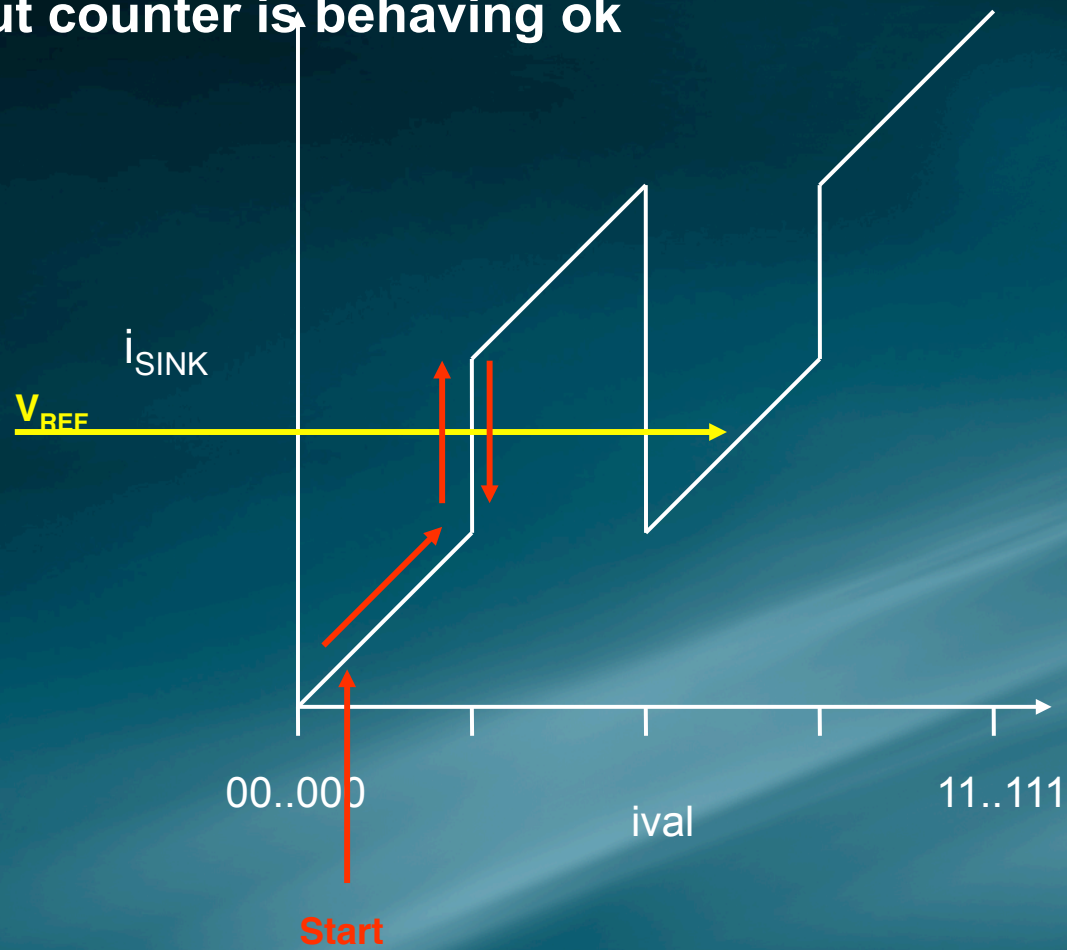
Incomplete Test Coverage

- Things operate smoothly within one quadrant.



Incomplete Value Checking

- Dither Amount is Too Big!
 - but counter is behaving ok



Modeling

- **Basic Model Requirement**
 - Analog output values reflect digital control.
 - Analog value can be checked.
- **Event-Driven**
 - Transition phenomena are of little interest when checking steady-state values.
- **Building blocks for digitally controlled electrical networks.**

Register Controlled Resistor



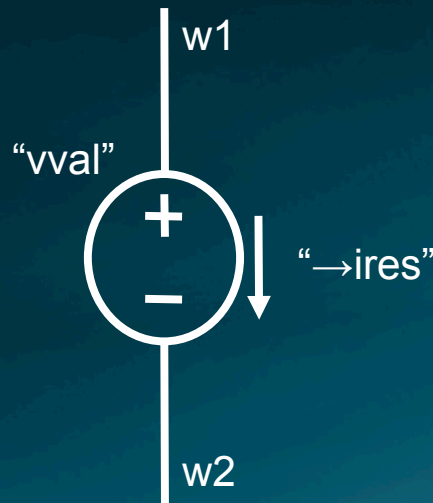
```
wire w1, w2;  
real rval;  
  
initial begin  
    rval = 100; // ohms  
    $resistor(w1, w2, rval);  
end
```

Register-Controlled Current Source



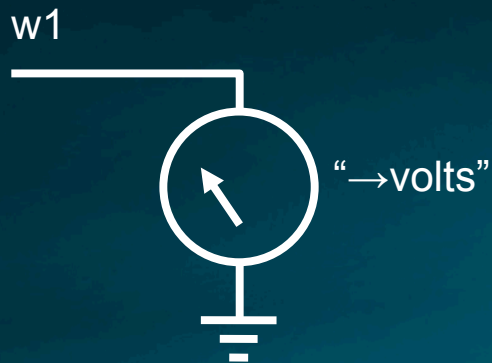
```
wire w1, w2;  
real cval;  
  
initial begin  
    cval = 0.1;  
    $csrc(w1, w2, cval);  
end
```

Register-Controlled Voltage Source



```
wire w1, w2;  
real vval;  
real ires;  
  
initial begin  
    vval = 2.0;  
    $vsrc(w1, w2, vval, ires);  
end
```

Voltage into a Register



```
wire w1;  
real volts;  
  
initial begin  
    $vprobe(w1, volts);  
end
```

Modeling the IDAC

```
module idac (inout wire out, input [5:0] ival);
```

```
    real isink;
```

```
    initial begin
```

```
        isink = 0.0; // initial current
```

```
        $csrc(out, GND, isink);
```

```
    end
```

```
    always @(ival)
```

```
        case (ival) // decode value
```

```
            5'b00000: isink = 0.1;
```

```
            5'b00001: isink = 0.15;
```

```
            ...
```

```
            5'b11111: isink = 1.65
```

```
        endcase
```

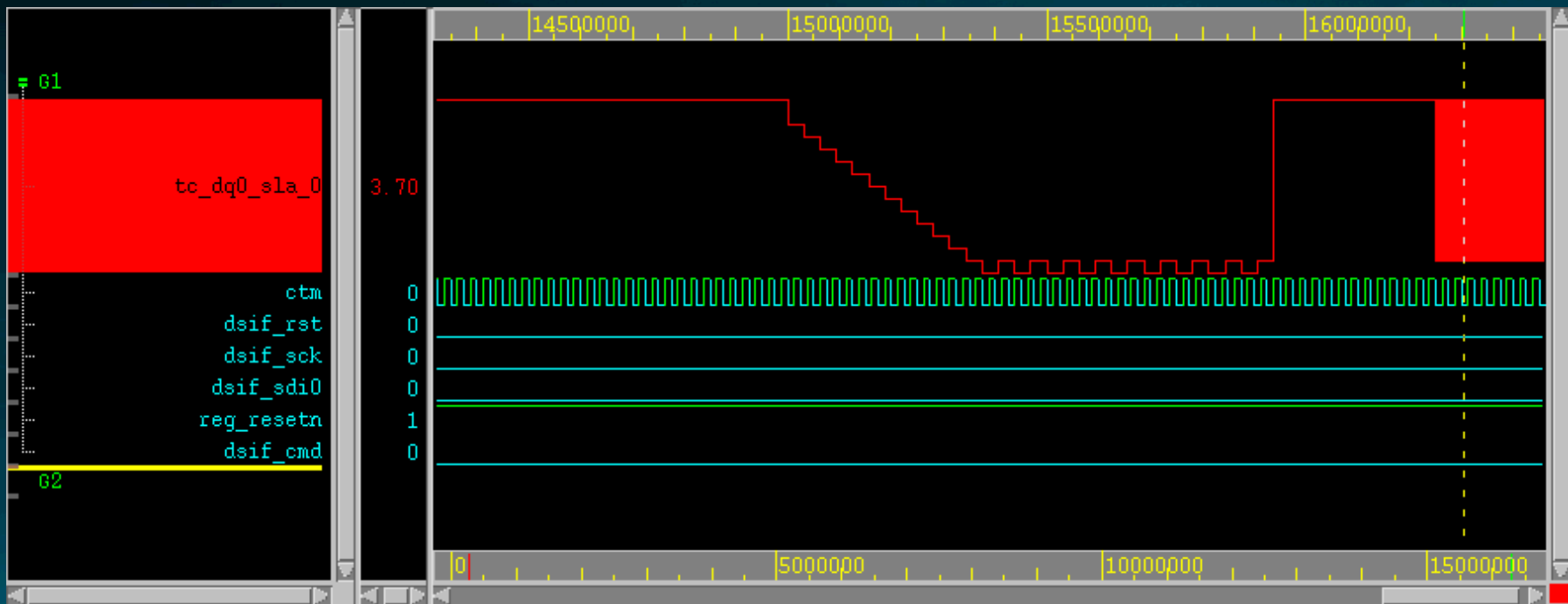
```
    endmodule
```

- induce a current with value “isink”

- Designer’s record of his understanding of decoding implemented by the analog block.

- A place to record
 - ones complement
 - twos complement
 - thermometer bits
 - illegal encodings

Piecewise-Constant Simulation Model



Correctness Criteria

- **The tracker moves in increments of one.**
- **The tracker settles on the two values surrounding the reference.**

Summary

- **Mixed-signal design verification requires appropriate “analog” abstract models.**
- **D/A interactions present unique challenges.**
- **Do check the output values of the analog blocks.**
 - **Do not restrict checking to outputs of decision elements.**